

Soyuz 3.0 SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 32

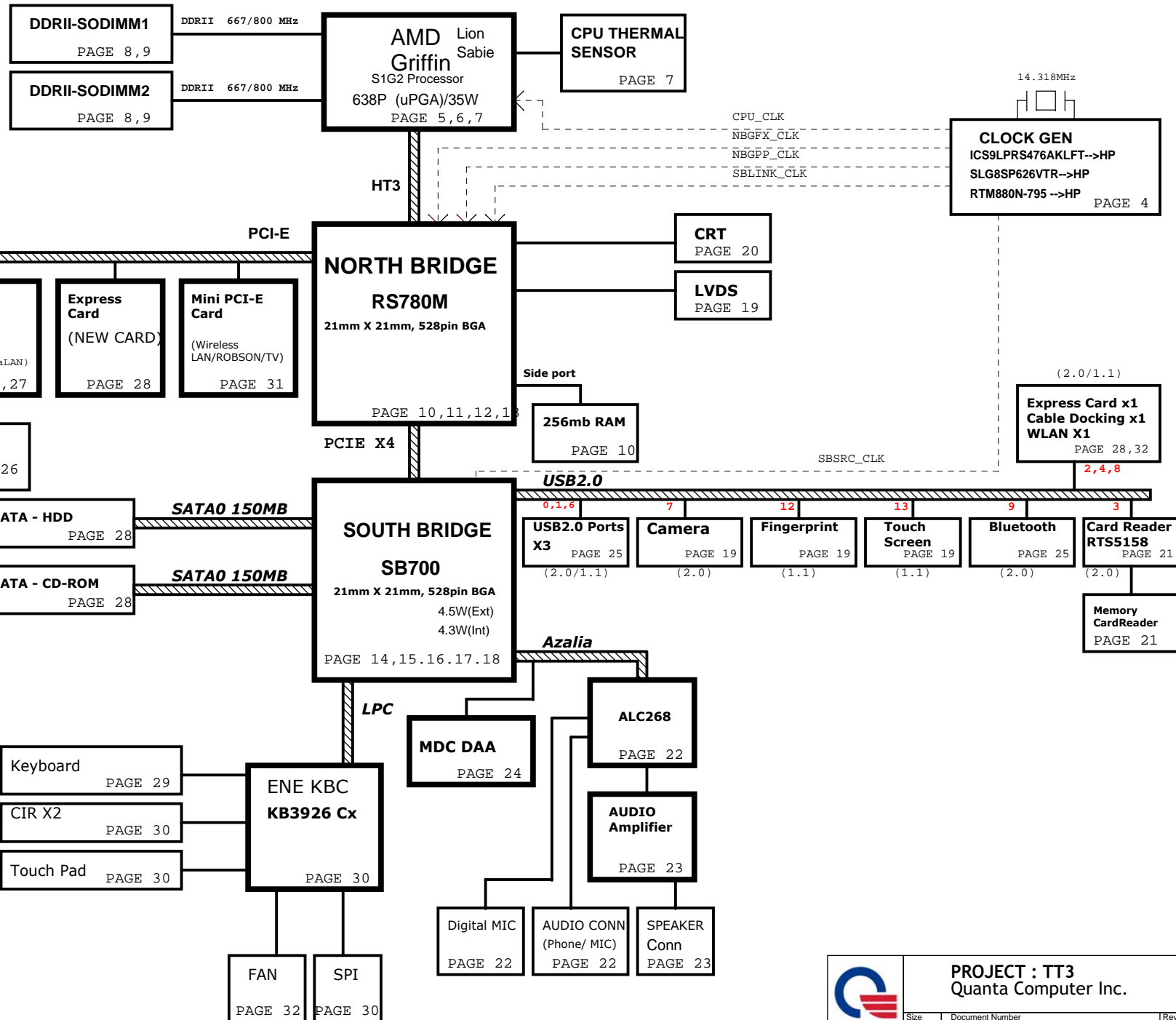
SYSTEM CHARGER(ISL6251A)
PAGE 39

SYSTEM POWER MAX1631A
PAGE 33

DDR II SMDDR_VTERM 1.8V/1.8VSUS
PAGE 36

VCCP +1.1V AND +1.2V(RT8204)
PAGE 34

CPU CORE ISL6265A
PAGE 35



Pg#	Description	NOTE
1	Schematic Block Diagram	
2	System Information	
3	Power sequence chart	
4	CLOCL GENERATOR	
5-7	AMD CPU S1G2 Griffin	
8-9	DDR II SO-DIMM	
10-13	RS780M	
14-18	SB700	
19	LCD CONNECTOR / LCD PWR / LID	
20	20--CRT,TV_OUT	
21	RTS5158E & CR SOCKET	
22	Azalia ALC268	
23	JACK/AMP_TPA0312	
24	Si3080 and MDC1.5 Connector	
25	Blue Tooth / USBX3 / TPM	
26	RTL8111C/RJ45	
27	LAN Power	
28	NEW CARD/SATA ODD/SATA HDD	
29	LED/KEYBOARD/SW	
30	KB3926/ROM/TP	
31	Mini CARD/Hole	
32	CABLE DOCKING/FAN	
33	3V/5V(MAX1631A)	
34	+1.2V/+1.1V (RT8204)	
35	+CPU_CORE ISL6265	
36	+1.8VSUS/+1.8V/+2.5V	
37	+1.1V/+1.2V_S5/+1.5V	
38	DISCHARGE	
39	Charger (ISL6251)	


* --> Un-stuff (ex. *1K/04)
 04-- 0402 footprint
 06-- 0603 footprint
 08-- 0805 footprint
 12-- 1206 footprint
 F-- 1% tolerance

Power & Ground

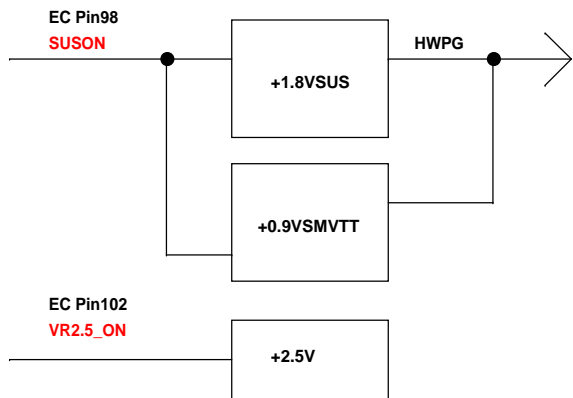
Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (18.5V)	
+BATT	S0, S3, S4, S5	MAIN BATTERY + (6.2V-8.4V)	
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3.3V)	
+12VALW	S0, S3, S4, S5	+12V	
+VCORE	S0	CPU CORE POWER (0.375-1.5V)	VRON
+CPUVDDNB	S0	CPU CORE POWER (1.375-1.5V)	VRON
+1.1V_NB	S0	+1.1 to +1.0 DYN	VRON
+1.1V	S0	+1.1V	VRON
+1.2VS5	S0, S3, S4, S5		S5_ON
+1.2V	S0	+1.2V	VRON
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
+5VSUS	S0, S3		SUSON
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+1.8V	S0		MAINON
+2.5V	S0	CPU VDDA	VR2.5_ON
+0.9VSMVTT	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
+0.9VSMVREF_DIMM	S0, S3	DDR REF POWER	SUSON
+AVDD	S0	AUDIO ANALOG POWER (5V)	MAINON
+3VLAVCC	S0, S3, S4, S5	LAN Power	LAN_ON
 GND	ALL PAGES	DIGITAL GROUND	
 AGND		AUDIO GND	

SMBUS	SMBUS function define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card (+3VS5)
SMBCLK2 SMBDAT2	New CARD (+3VS5)

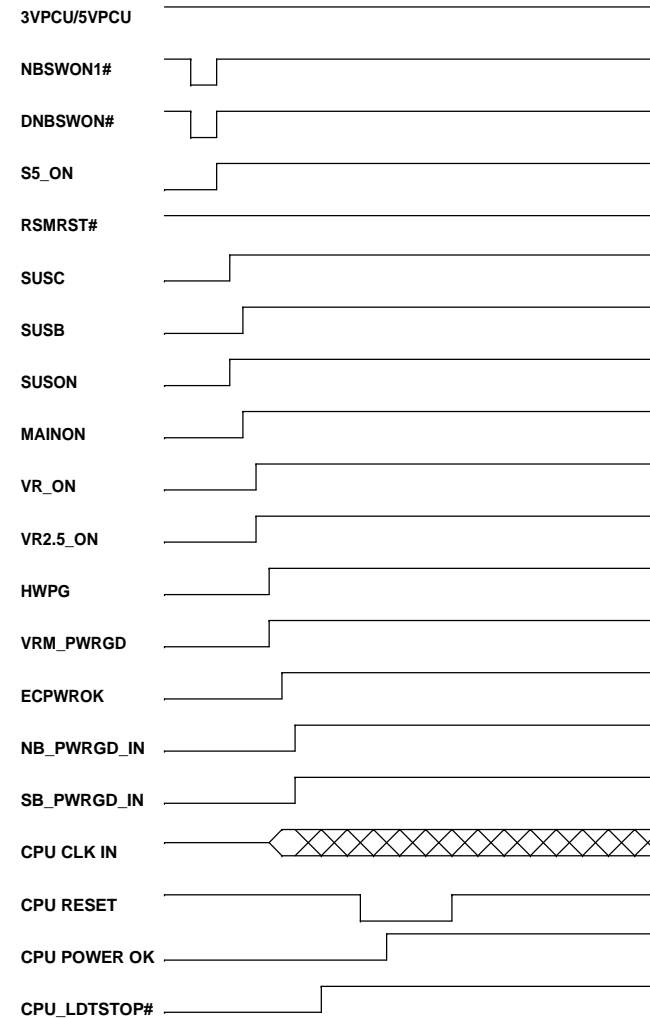
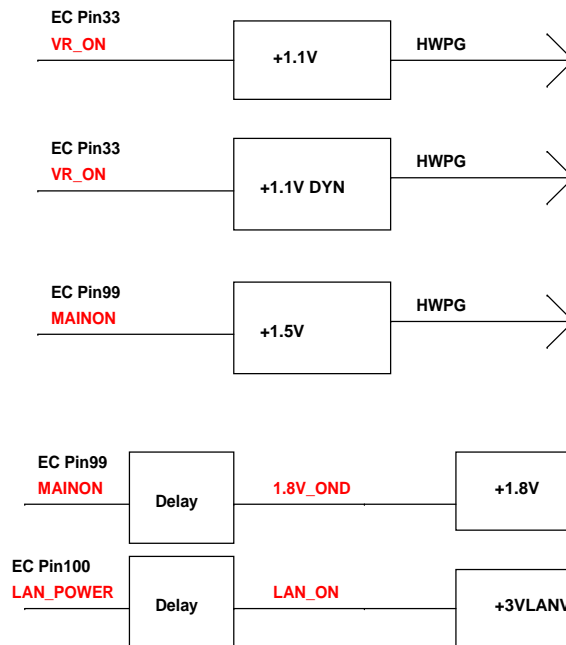
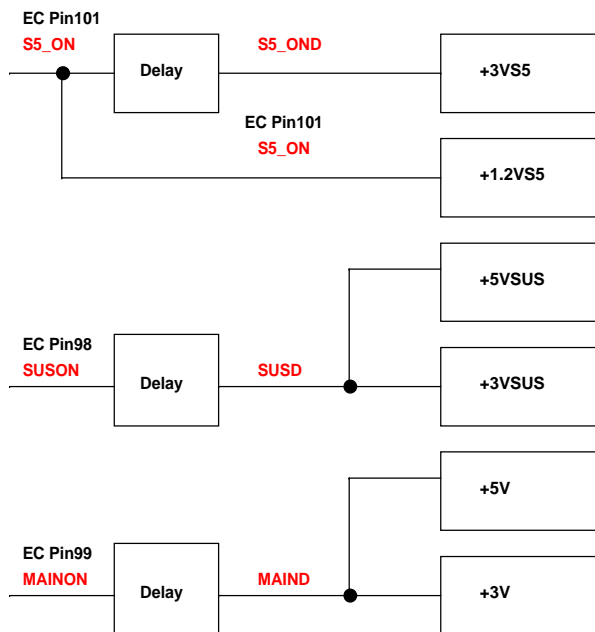
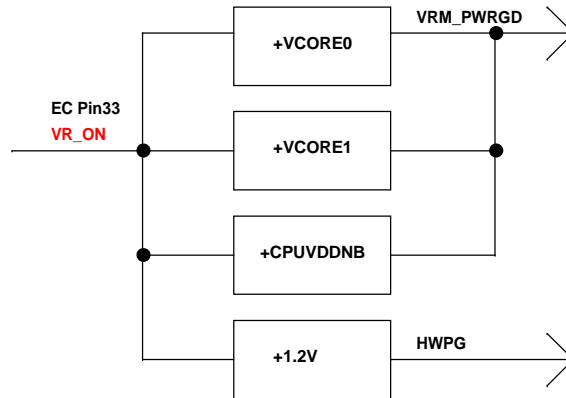
02

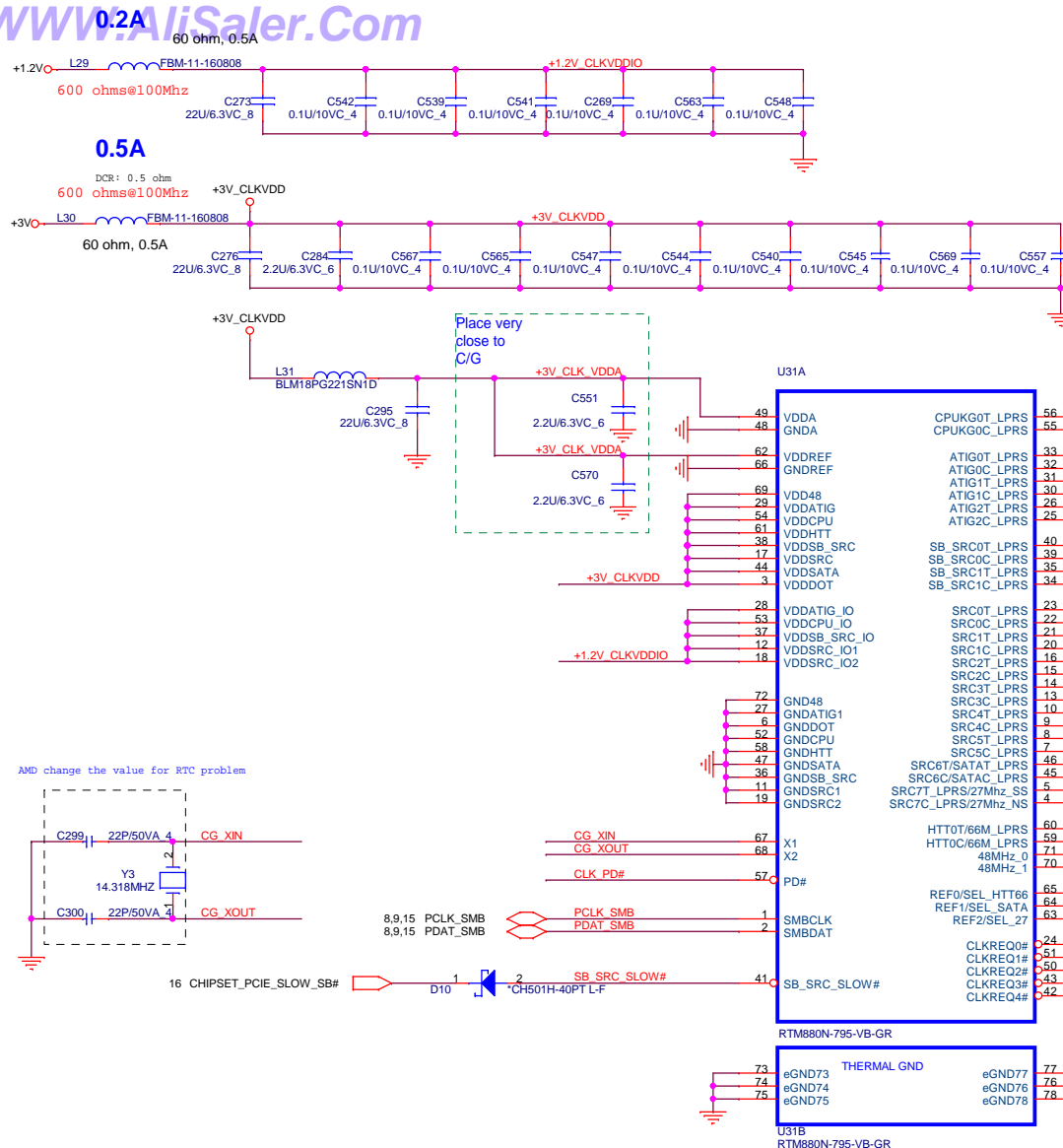
 NB5/RD2/HW1	PROJECT : TT3 Quanta Computer Inc.	
	Size Custom Document Number System Information	Date: Wednesday, August 27, 2008 Sheet 2 of 41

CPU Power Group A



CPU Power Group B



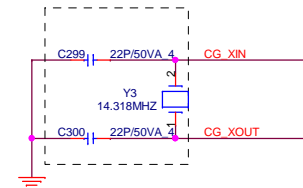


Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

AMD change the value for RTC problem



16 CHIPSET_PCIE_SLOW_SB#

8,9,15 PCLK_SMB
8,9,15 PDAT_SMB

PCLK_SMB
PDAT_SMB

* default

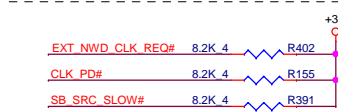
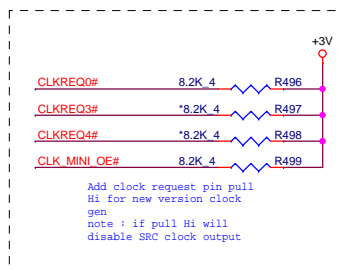
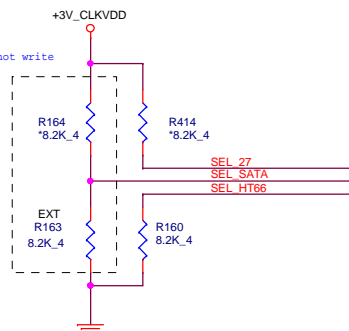
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	0	100 MHz spreading differential SRC clock
	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will be configured as input mode, BIOS can program it to output mode.

+1.2V 5,13,14,16,17,34,37
+3V 5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

Wrong type bios can not write

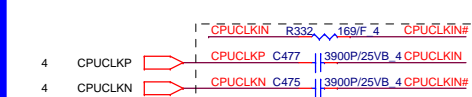
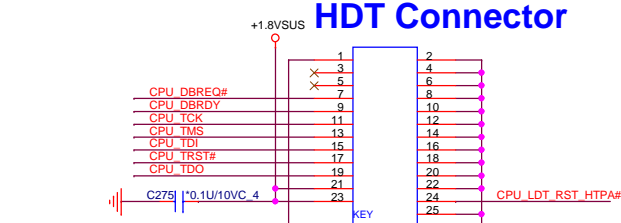
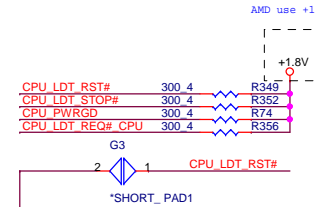
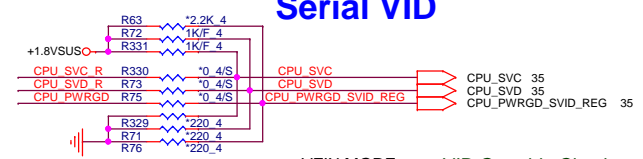
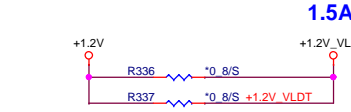


PROJECT : TT3
Quanta Computer Inc.

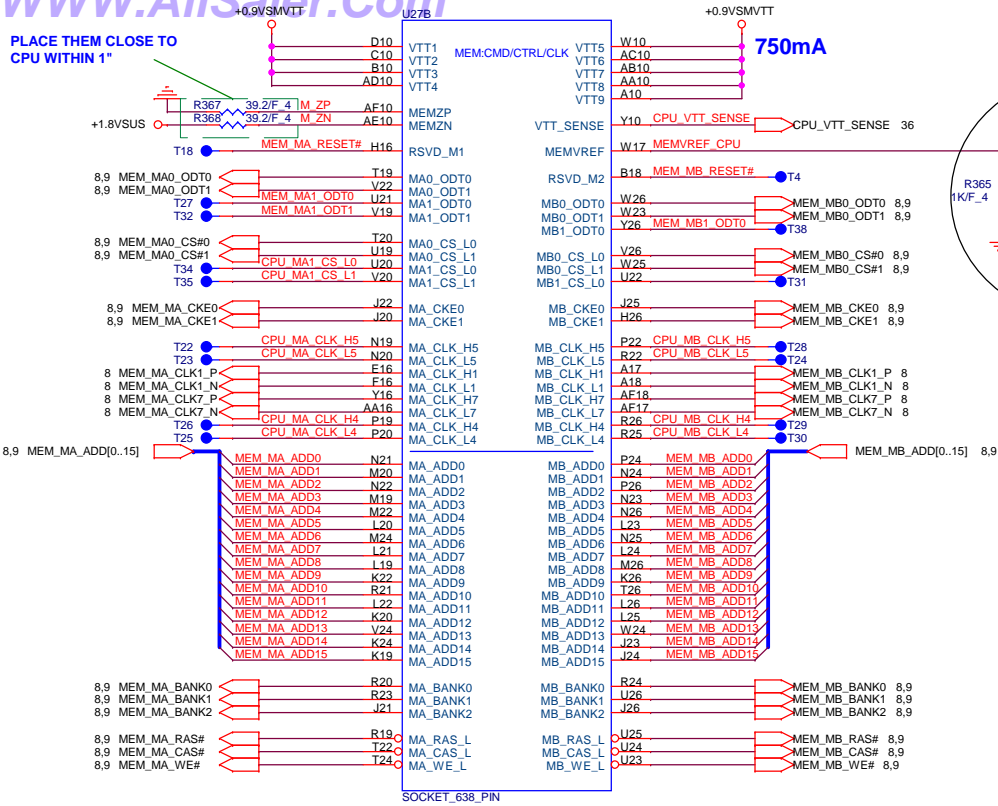
Size Custom	Document Number Clock generator	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 4 of 41	



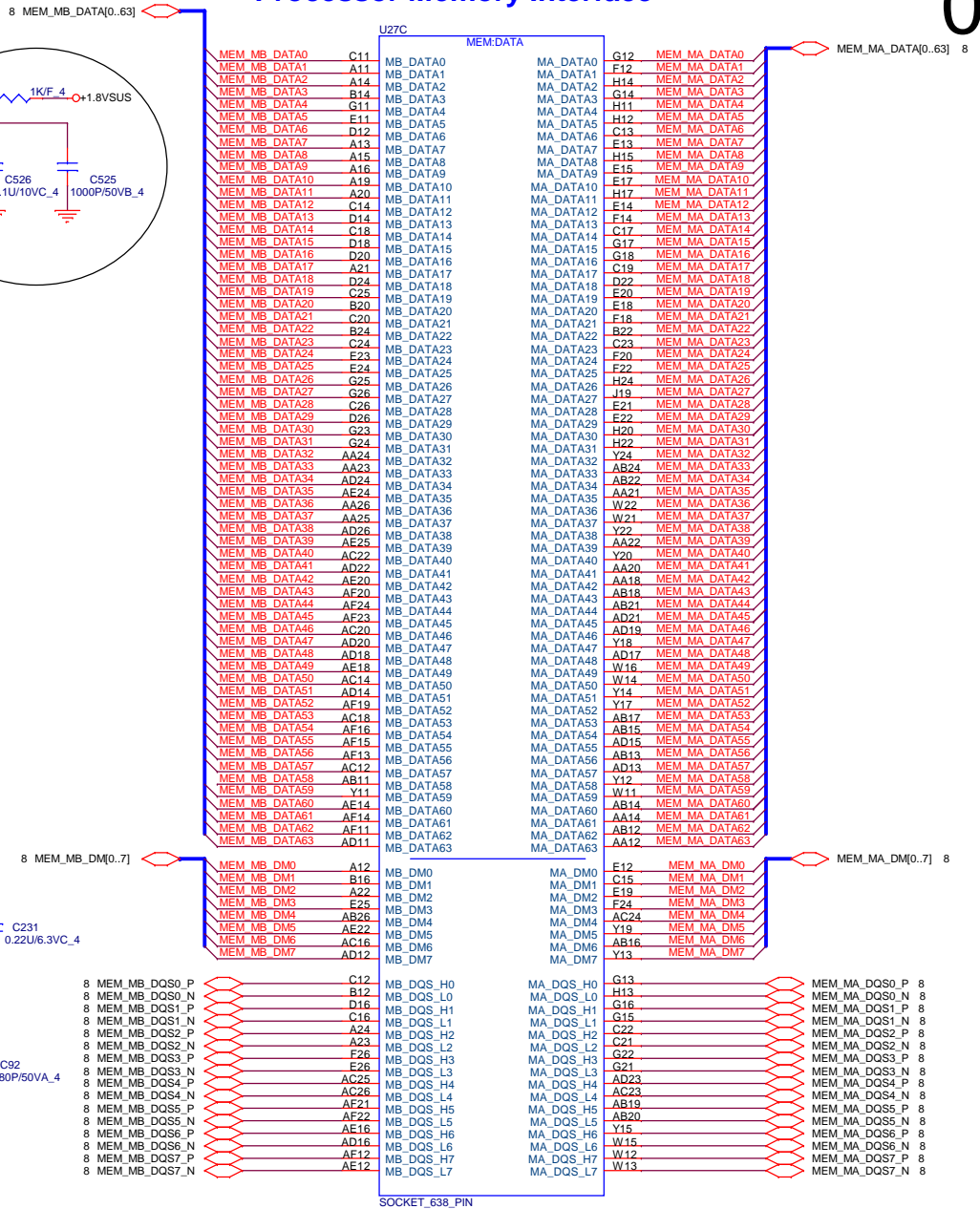
250mA



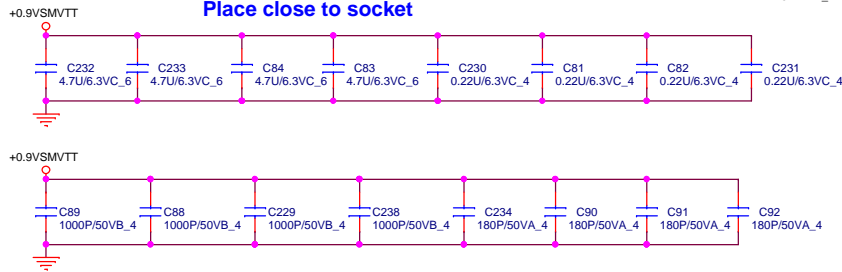
PLACE THEM CLOSE TO CPU WITHIN 1"



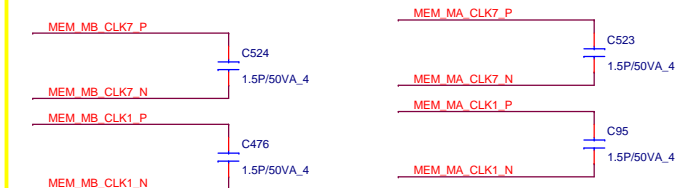
Processor Memory Interface



Place close to socket



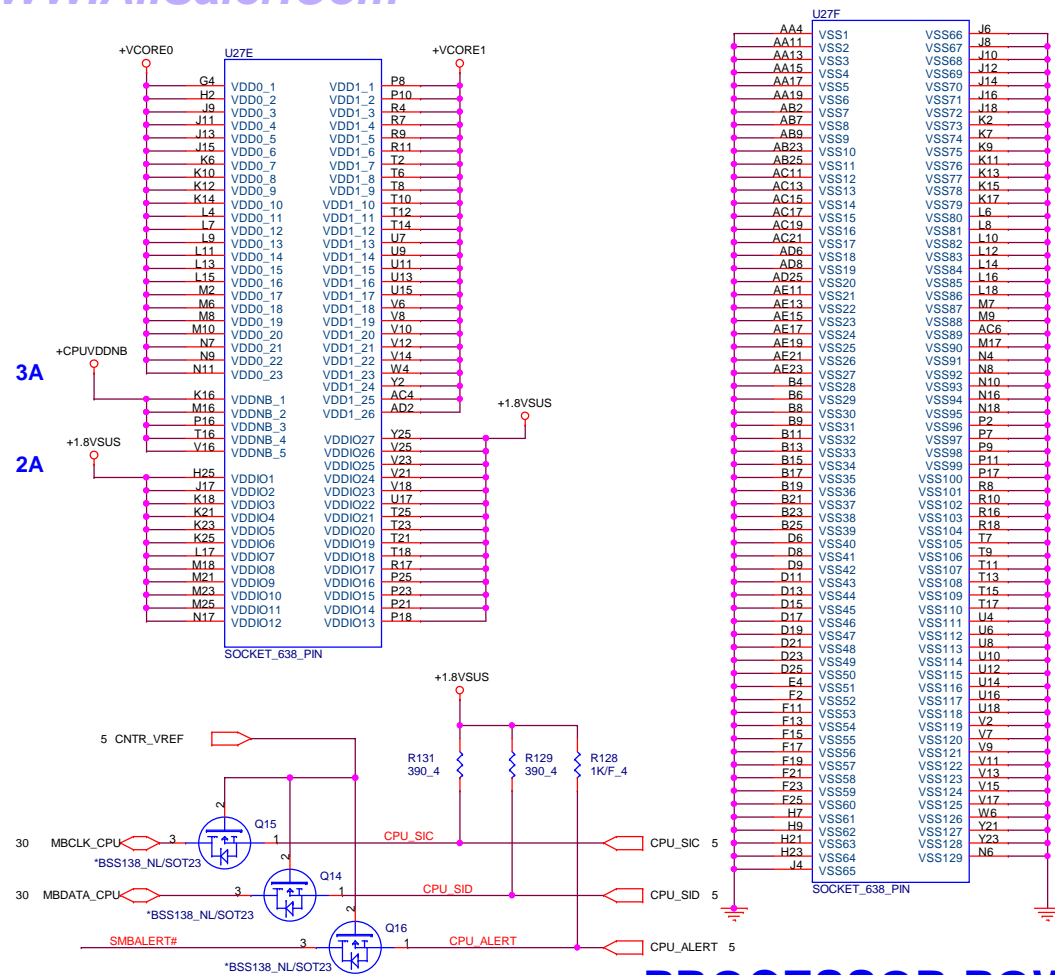
Close to CPU within 1500 mls



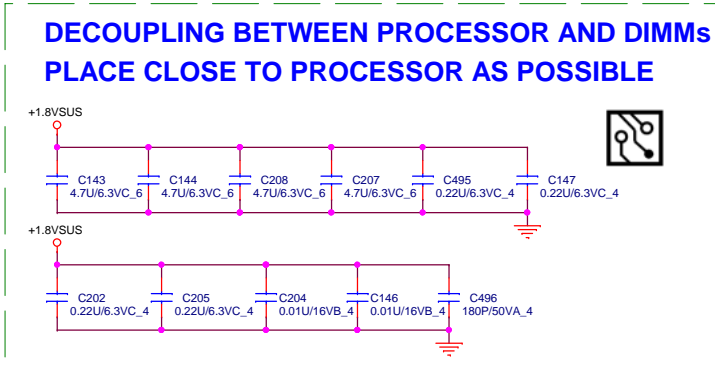
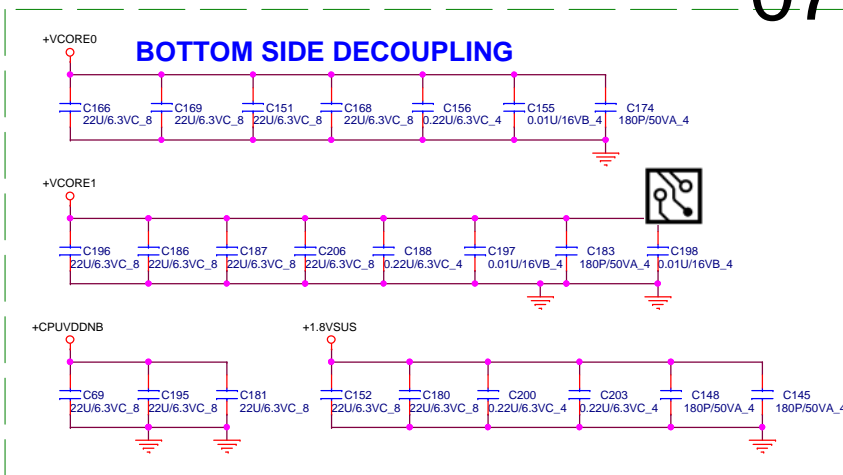
+0.9VSMVTT 9,31,36
+1.8VSUS 5,7,8,9,31,35,36,37



PROJECT : TT3
Quanta Computer Inc.



PROCESSOR POWER AND GROUND



+VCORE0 35
+VCORE1 35
+CPUVDDNB 35
1.8VSUS 5,6,8,9,31,35,36,37
4,5,9,12,13,15,16,18,19,20,22,23,26,28,29,30,31,33,34,38

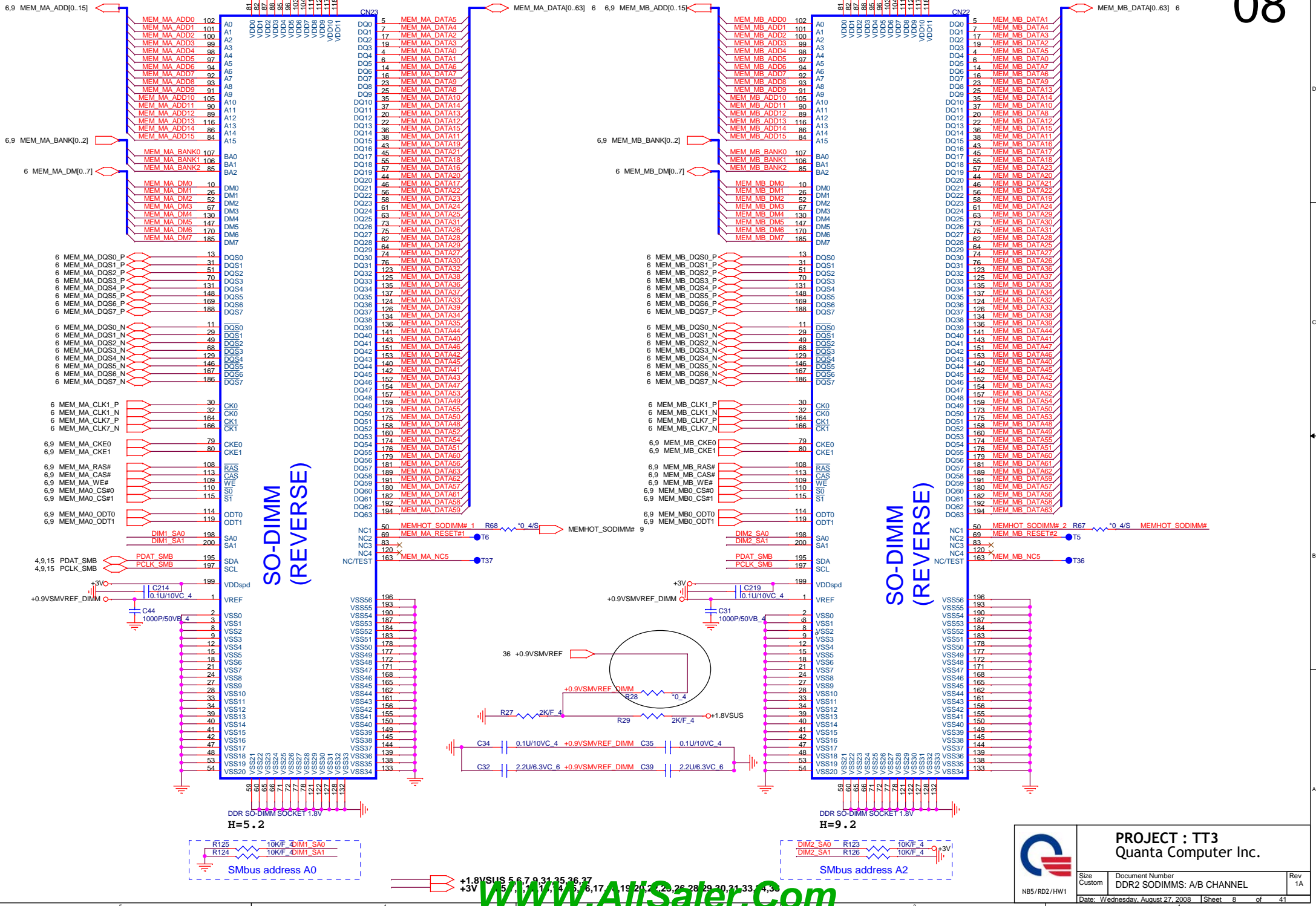


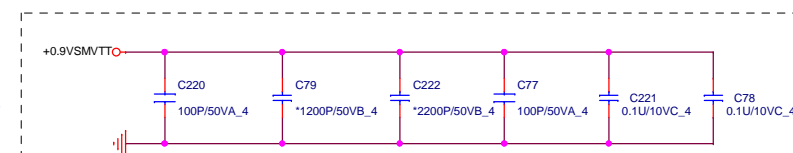
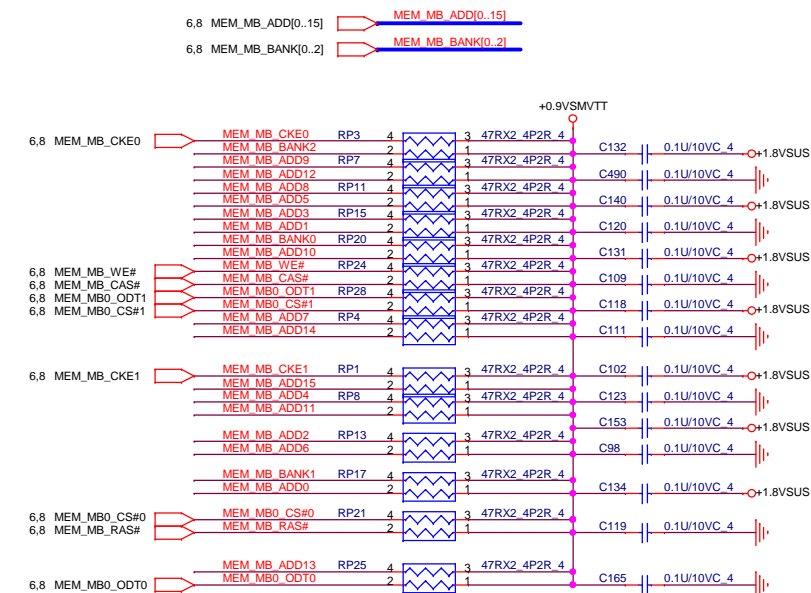
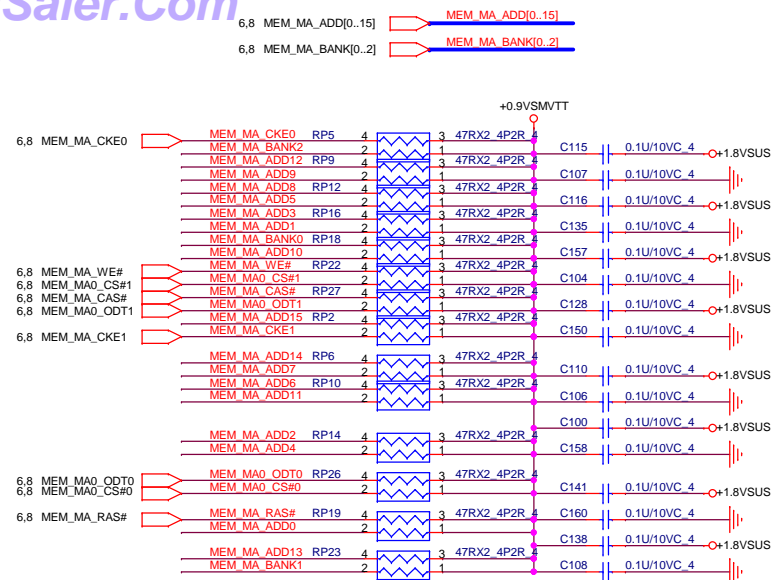
PROJECT : TT3
Quantas Computer Inc.

Size Custom Document Number S1G2 PWR & GND 3/3

Rev 1A

Date: Wednesday, August 27, 2008 Sheet 7 of 41





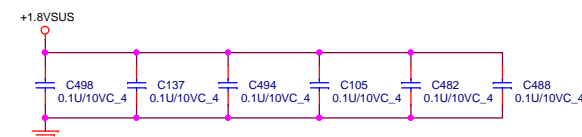
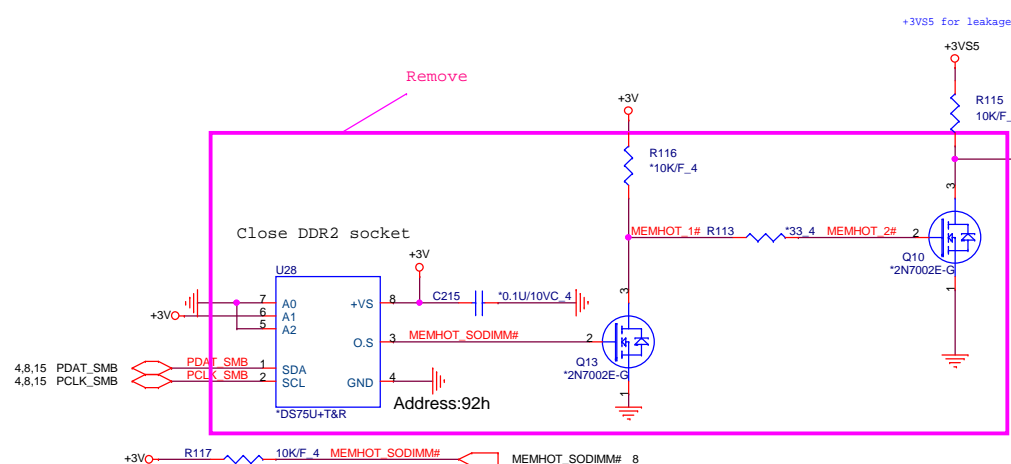
Emi request



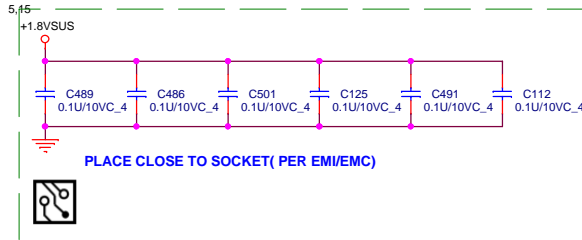
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO SOCKET(PER EMI/EMC)



PLACE CLOSE TO SOCKET(PER EMI/EMC)

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	Y22	HT_RXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	E24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	E25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	E23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	E22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	K22	HT_NB_CPU_CAD_L7

PART 1 OF 6

HYPER TRANSPORT CPU I/F

follow AMD
check list to
change part
number 300 ohm
to 301 ohm

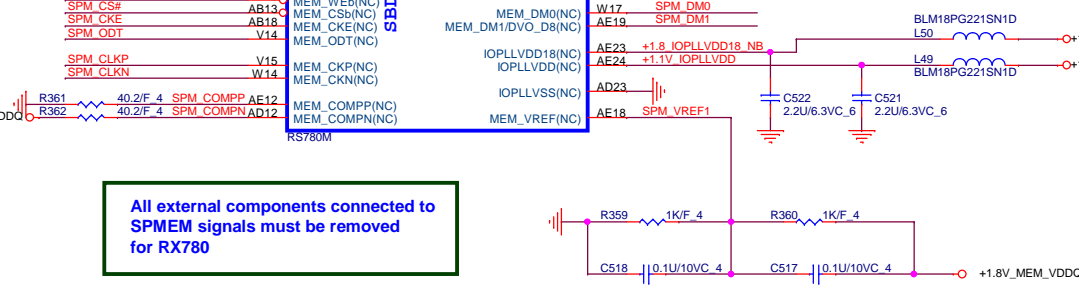
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DV0_VSYN(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DV0_HSYN(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DV0_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DV0_D0(NC)	V17	SPM_DQ3
SPM_A4	AE12	MEM_A4(NC)	MEM_DQ4(NC)	AA17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DV0_D1(NC)	V17	SPM_DQ5
SPM_A6	AD14	MEM_A6(NC)	MEM_DQ6/DV0_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD13	MEM_A7(NC)	MEM_DQ7/DV0_D3(NC)	Y15	SPM_DQ7
SPM_A8	AD15	MEM_A8(NC)	MEM_DQ8/DV0_D4(NC)	AC20	SPM_DQ8
SPM_A9	AC16	MEM_A9(NC)	MEM_DQ9/DV0_D5(NC)	AD19	SPM_DQ9
SPM_A10	AE13	MEM_A10(NC)	MEM_DQ10/DV0_D6(NC)	AC18	SPM_DQ10
SPM_A11	AC14	MEM_A11(NC)	MEM_DQ11/DV0_D7(NC)	AD22	SPM_DQ11
SPM_A12	Y14	MEM_A12(NC)	MEM_DQ12/DV0_D8(NC)	AD22	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DV0_D9(NC)	AD21	SPM_DQ13
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ14/DV0_D10(NC)	AC22	SPM_DQ14
SPM_BA1	AE17	MEM_BA1(NC)	MEM_DQ15/DV0_D11(NC)	AD21	SPM_DQ15
SPM_BA2	AD17	MEM_BA2(NC)	MEM_DQ16/DV0_D12(NC)		
SPM_RAS#	W12C	MEM_RASb(NC)	MEM_DQ17/DV0_D13(NC)	Y17	SPM_DQ16
SPM_CAS#	Y12C	MEM_CASb(NC)	MEM_DQ18/DV0_D14(NC)	W18	SPM_DQ17
SPM_WE#	AD18C	MEM_WEb(NC)	MEM_DQ19/DV0_D15(NC)	AD20	SPM_DQ18
SPM_CS#	AB13C	MEM_CSb(NC)	MEM_DQ20/DV0_D16(NC)	AE21	SPM_DQ19
SPM_CKE	AB18C	MEM_CKEb(NC)	MEM_DQ21/DV0_D17(NC)	W17	SPM_DQ20
SPM_ODT	V14	MEM_ODT(NC)	MEM_DQ22/DV0_D18(NC)	AE19	SPM_DQ21
SPM_CLKP	W15	MEM_CLKP(NC)	MEM_DQ23/DV0_D19(NC)	AE23	SPM_DQ22
SPM_CLKN	W14	MEM_CLKN(NC)	MEM_DQ24/DV0_D20(NC)	AE24	SPM_DQ23

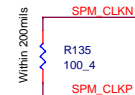
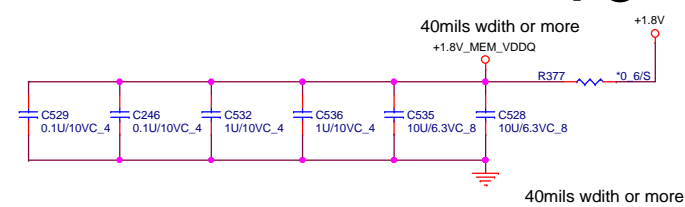
PART 4 OF 6

SBD_MEM/DV0_I/F

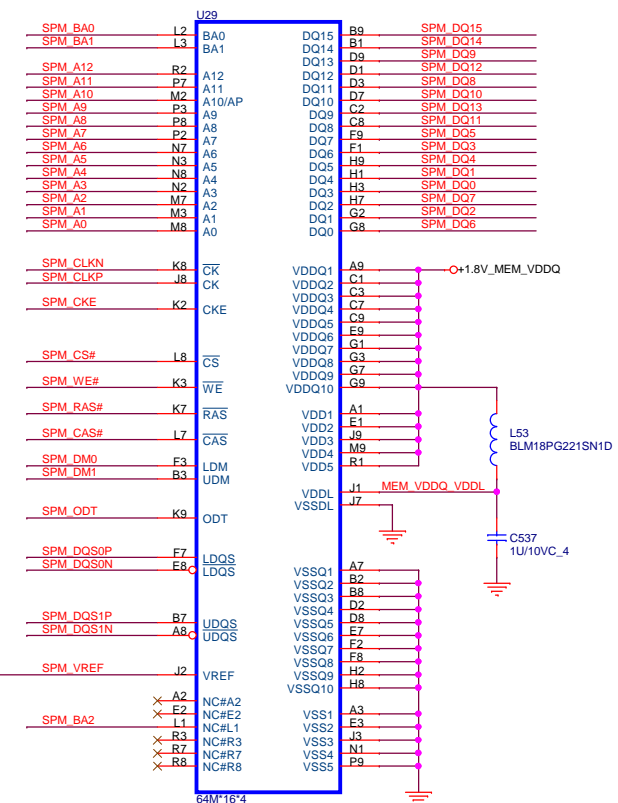
All external components connected to
SPMEM signals must be removed
for RX780

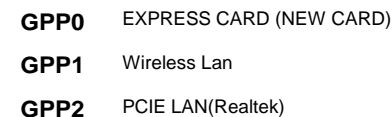


HT_CPU_NB_CAD_H[15..0]	HT_CPU_NB_CAD_H[15..0]	5
HT_CPU_NB_CAD_L[15..0]	HT_CPU_NB_CAD_L[15..0]	5
HT_CPU_NB_CLK_H[1..0]	HT_CPU_NB_CLK_H[1..0]	5
HT_CPU_NB_CLK_L[1..0]	HT_CPU_NB_CLK_L[1..0]	5
HT_CPU_NB_CTL_H[1..0]	HT_CPU_NB_CTL_H[1..0]	5
HT_CPU_NB_CTL_L[1..0]	HT_CPU_NB_CTL_L[1..0]	5
HT_NB_CPU_CAD_H[15..0]	HT_NB_CPU_CAD_H[15..0]	5
HT_NB_CPU_CAD_L[15..0]	HT_NB_CPU_CAD_L[15..0]	5
HT_NB_CPU_CLK_H[1..0]	HT_NB_CPU_CLK_H[1..0]	5
HT_NB_CPU_CLK_L[1..0]	HT_NB_CPU_CLK_L[1..0]	5
HT_NB_CPU_CTL_H[1..0]	HT_NB_CPU_CTL_H[1..0]	5
HT_NB_CPU_CTL_L[1..0]	HT_NB_CPU_CTL_L[1..0]	5



Close to U23

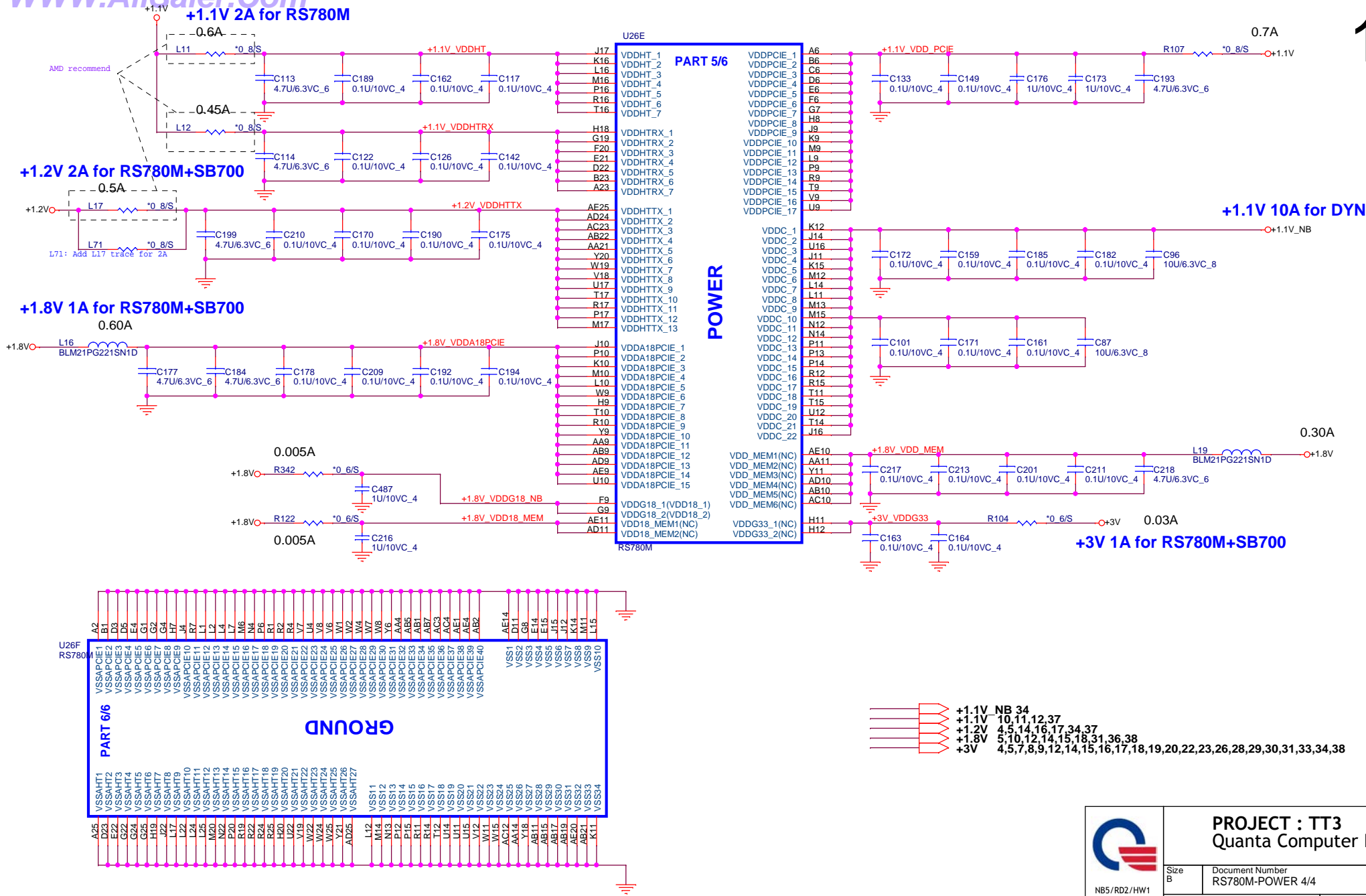




> +1.1V 10,12,13,37



Size B	Document Number RS780M-PCIE I/F 2/4	Rev 1A
Date: Wednesday, August 27, 2008		Sheet 11 of 41



PROJECT : TT3
Quanta Computer Inc.

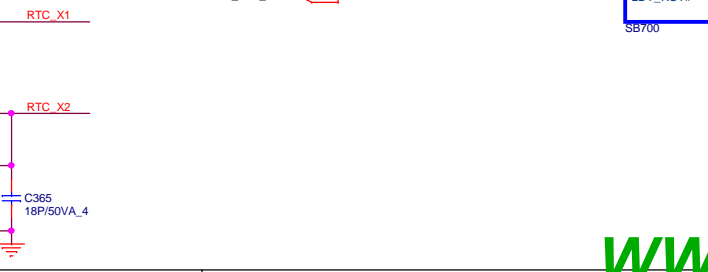
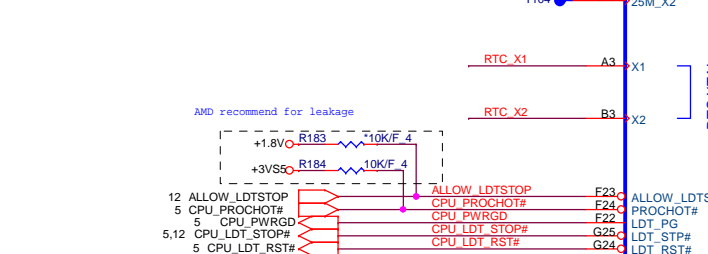
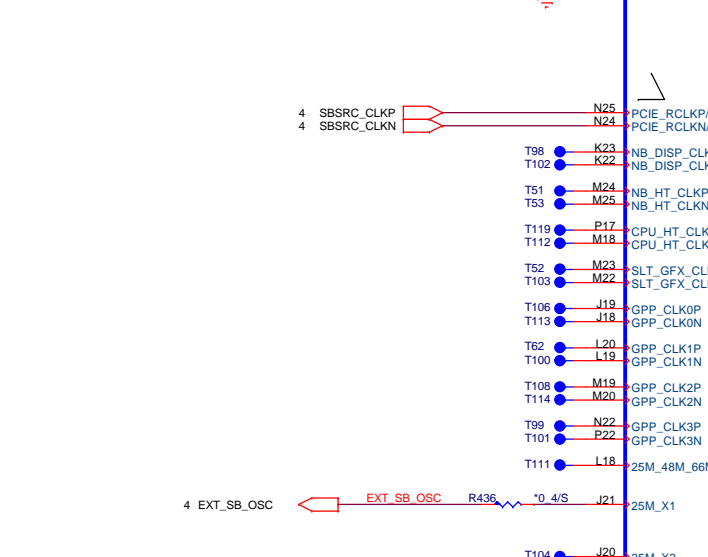
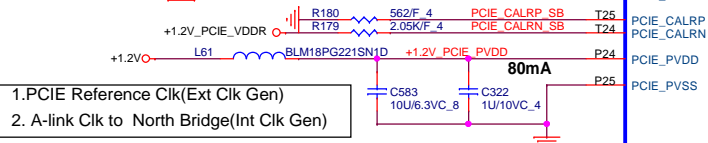
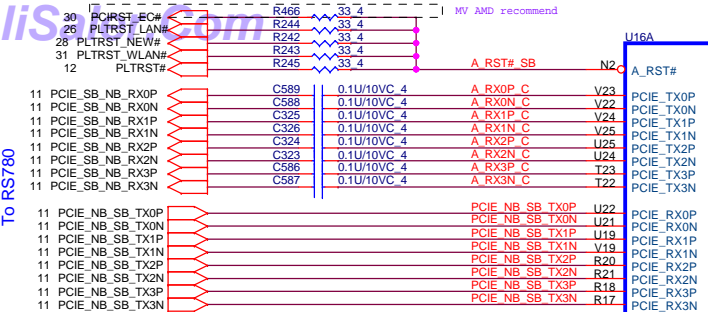
Size B	Document Number RS780M-POWER 4/4	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 13 of 41	

PLACE THESE
PCIe AC
COUPLING CAPS
CLOSE TO U600



To RS780

1. PCIe Reference Clk (Ext Clk Gen)
2. A-link Clk to North Bridge (Int Clk Gen)



SB700
Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

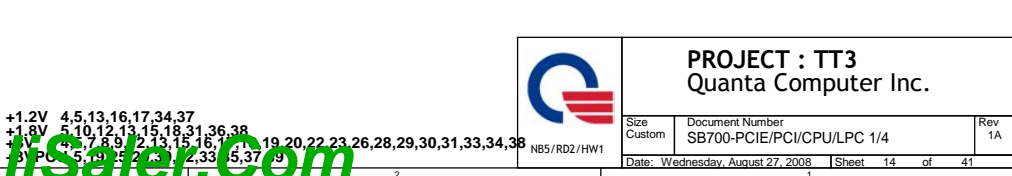
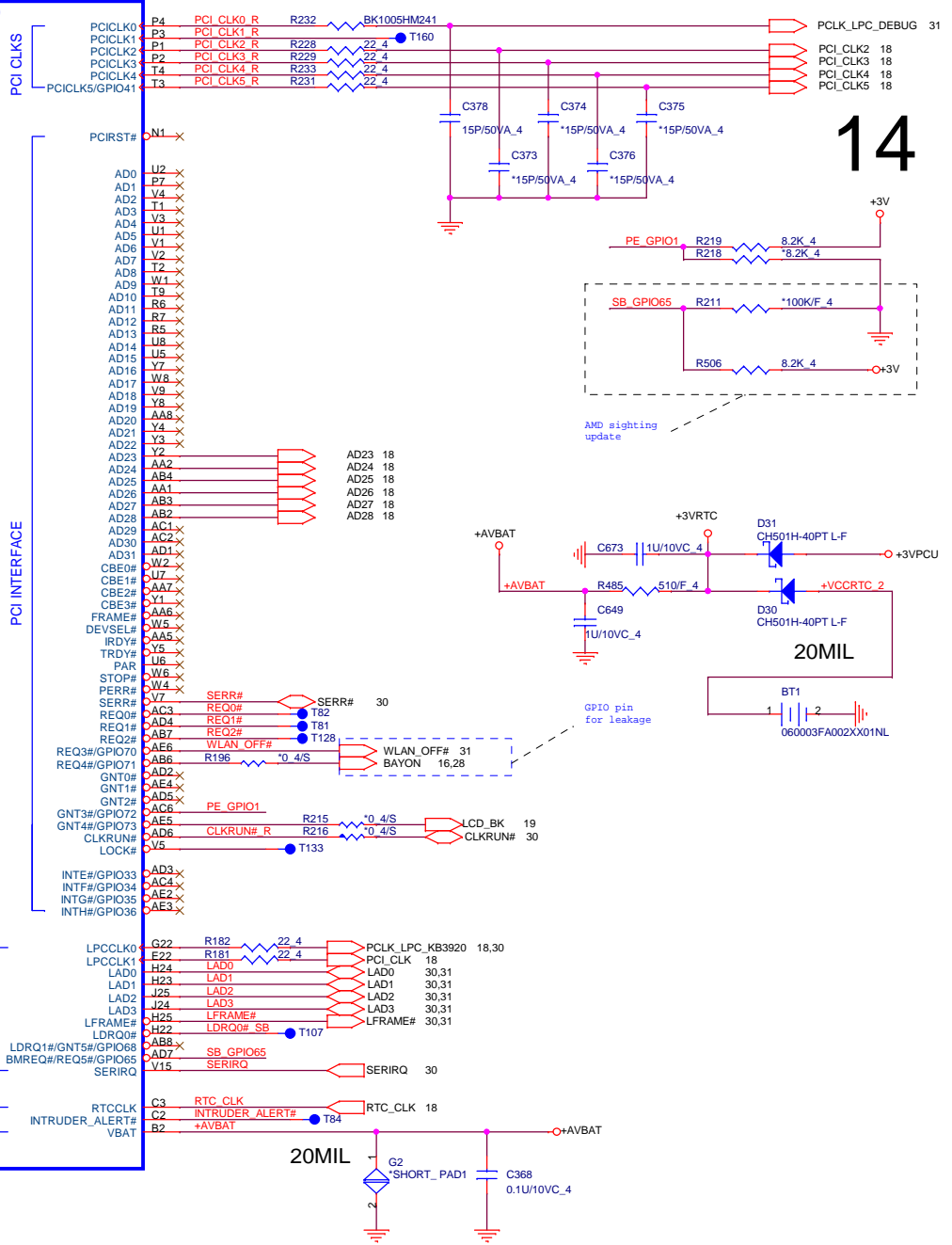
CLOCK GENERATOR

LPC

RTC

CPU

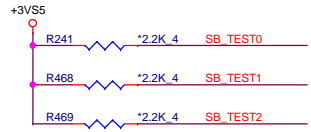
SB700



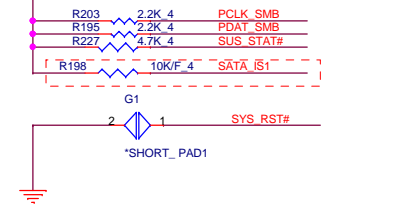
PROJECT : TT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-PCIe/PCI/CPU/LPC 1/4	1A
Date: Wednesday, August 27, 2008	Sheet 14 of 41	

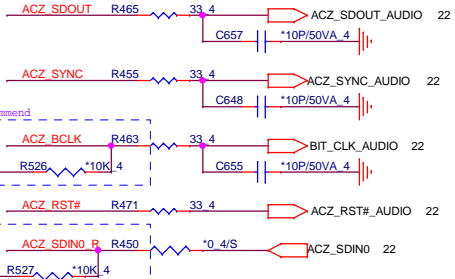
SB700 SBTEST0/1/2 has internal 10K PD.



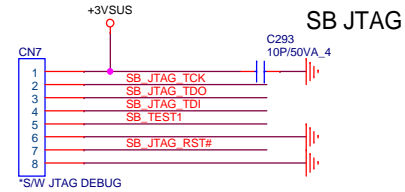
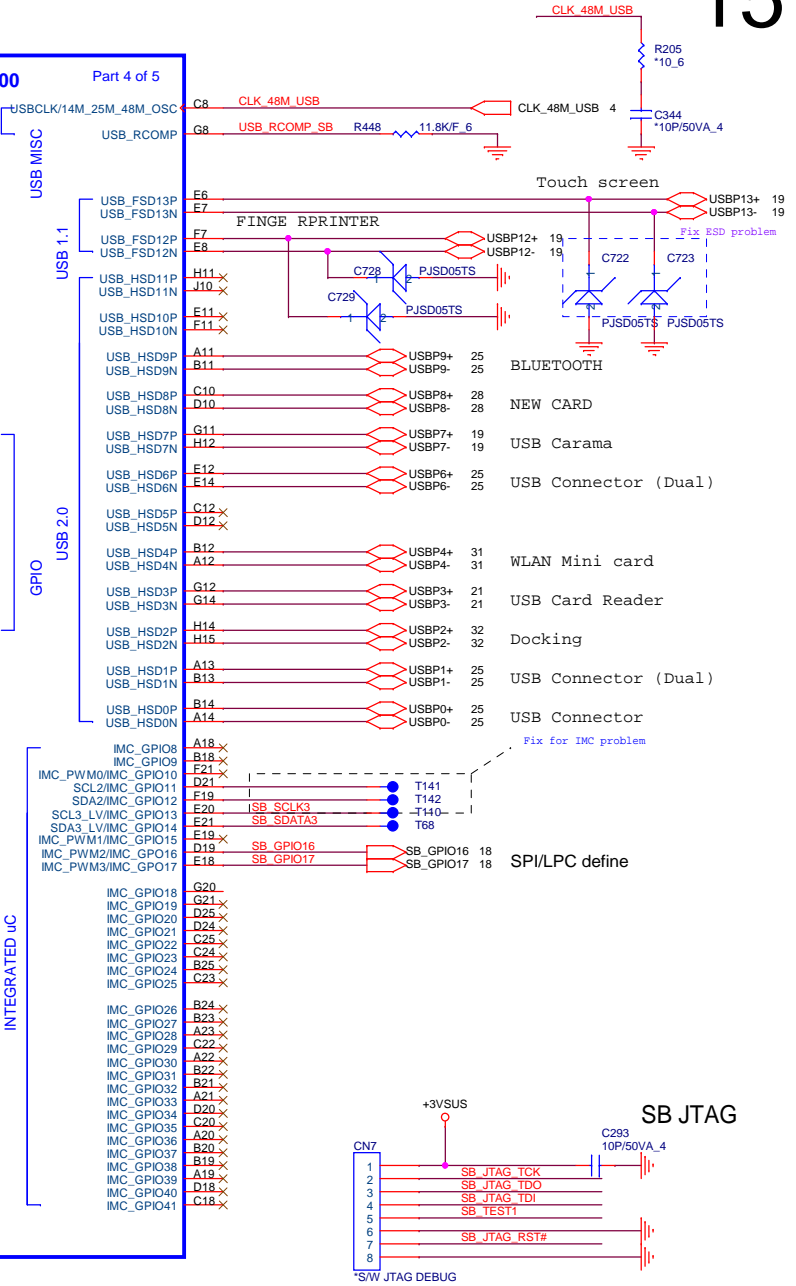
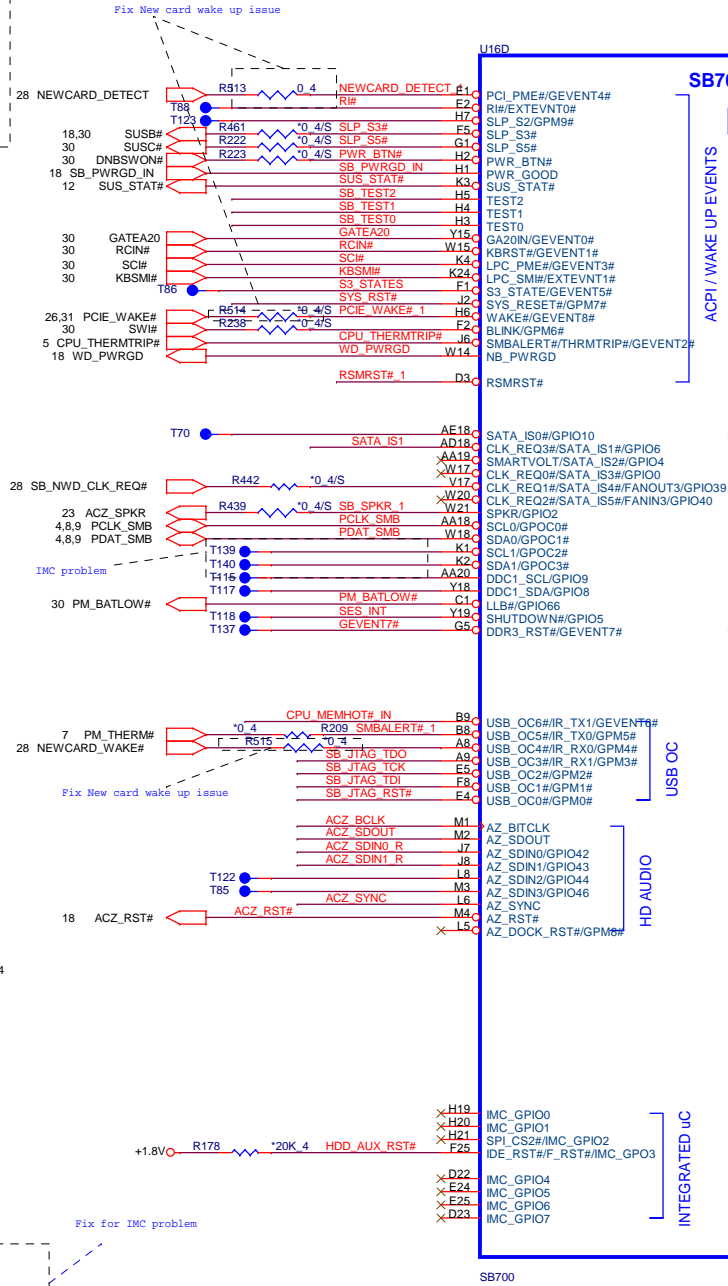
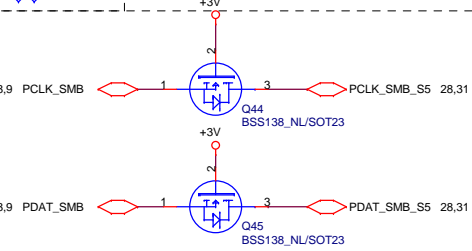
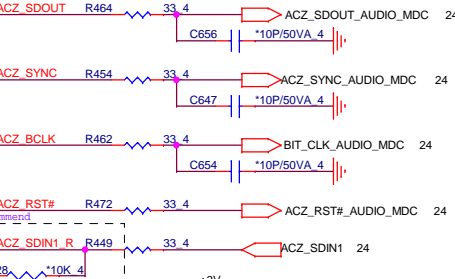
For SATA ODD hot plug



To Azalia



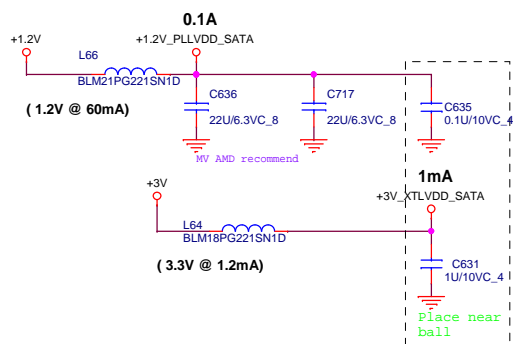
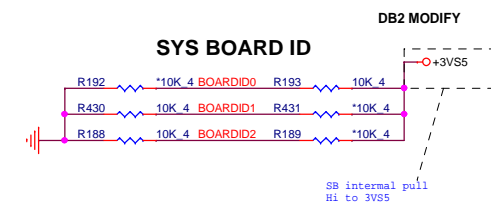
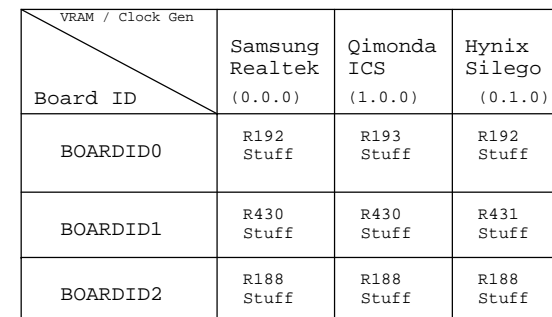
To Modem Board



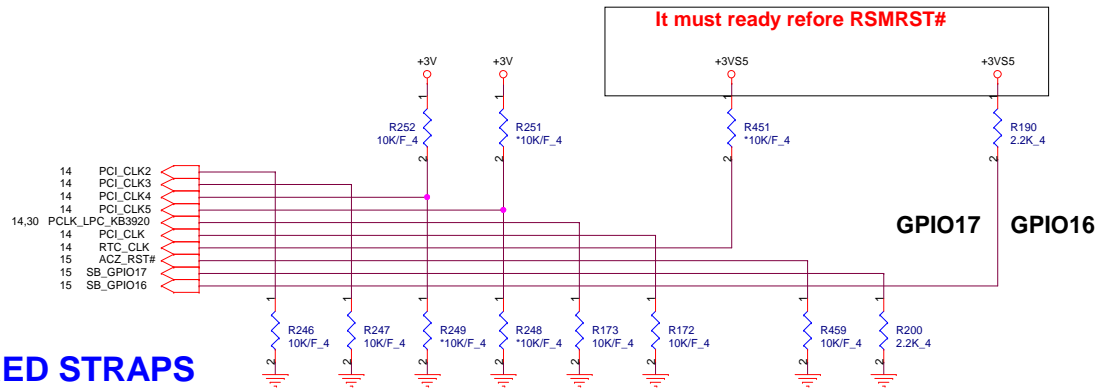
+1.8VSUS 5,6,7,8,9,31,35,36,37
+1.8VSUS 10,12,13,14,18,31,36,38
+3VSUS 21,24,25,29,31,33,34,35,36,38
+3VSUS 9,14,16,17,18,28,33,38
+3V 4,5,7,8,9,12,13,14,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38



PROJECT : TT3
Quanta Computer Inc.





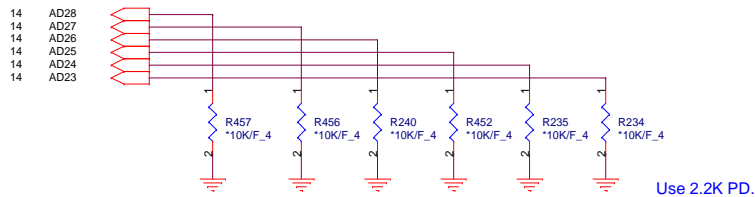


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

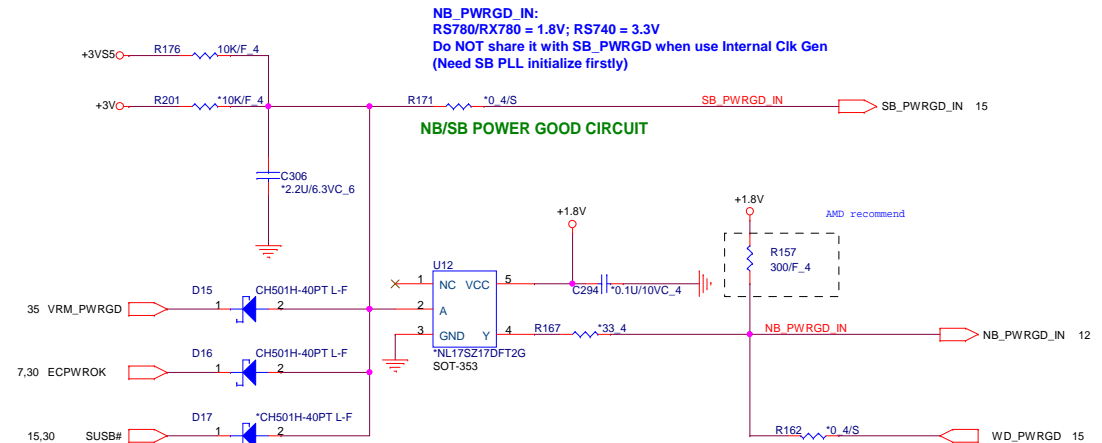
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCLK_LPC_KB3920	PCI_CLK	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM	DEFAULT

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

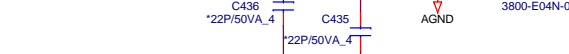
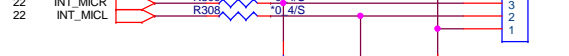
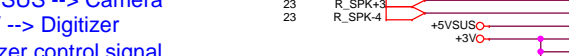
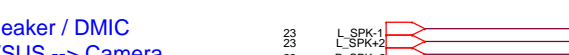
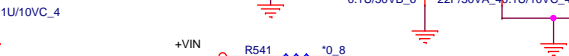
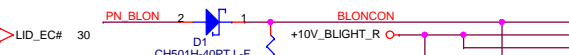
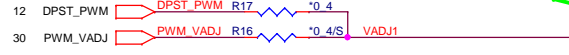
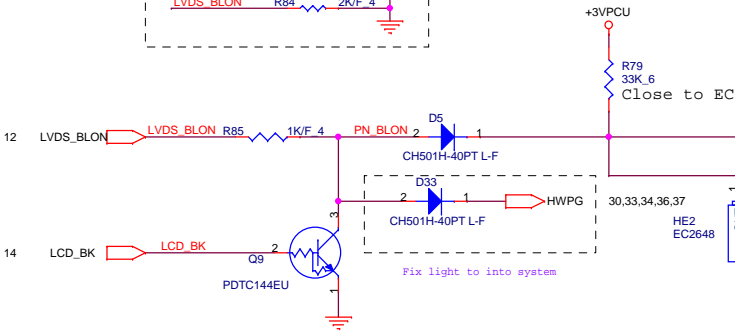
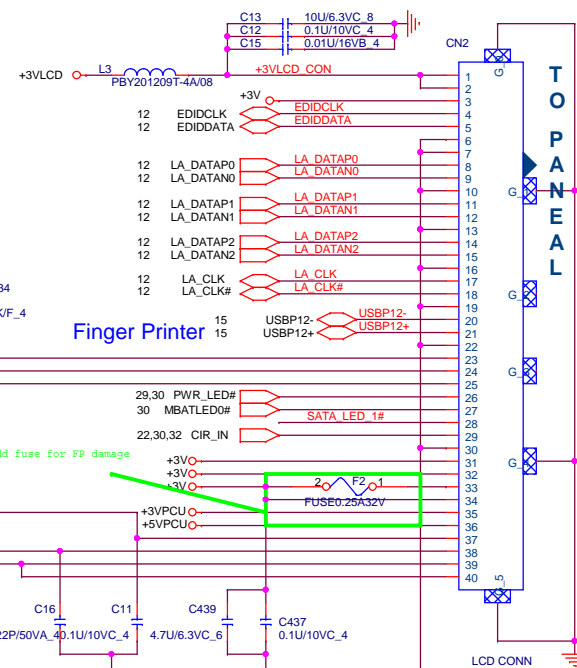
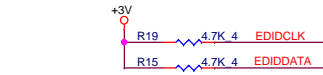
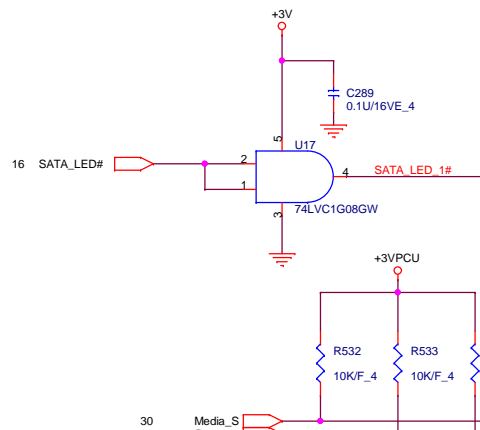
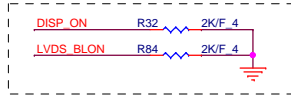
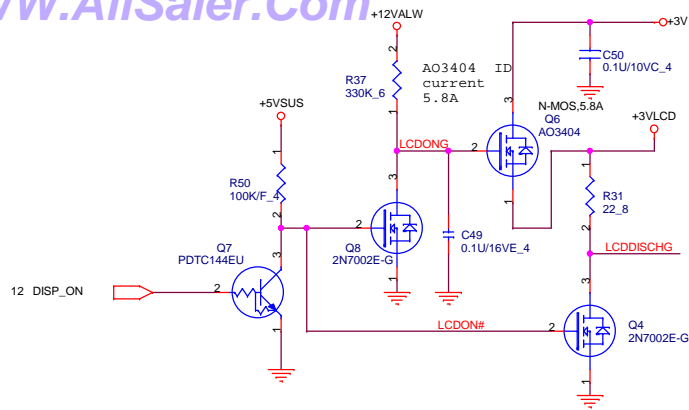


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : TT3
Quanta Computer Inc.

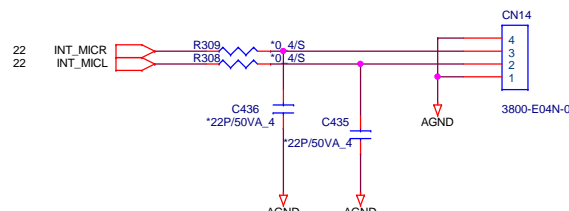
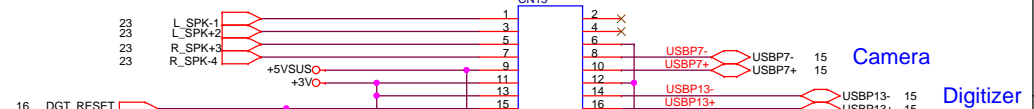
Size Custom	Document Number SB700-STRAPS,PWRGD	Rev 1A
Date: Wednesday, August 27, 2008 Sheet 18 of 41		

+1.8V 5,10,12,13,14,15,31,36,38
+3V 4,5,7,8,9,12,13,14,15,16,17,19,20,22,23,26,28,29,30,31,33,34,38
+3VS5 9,14,15,16,17,28,33,38



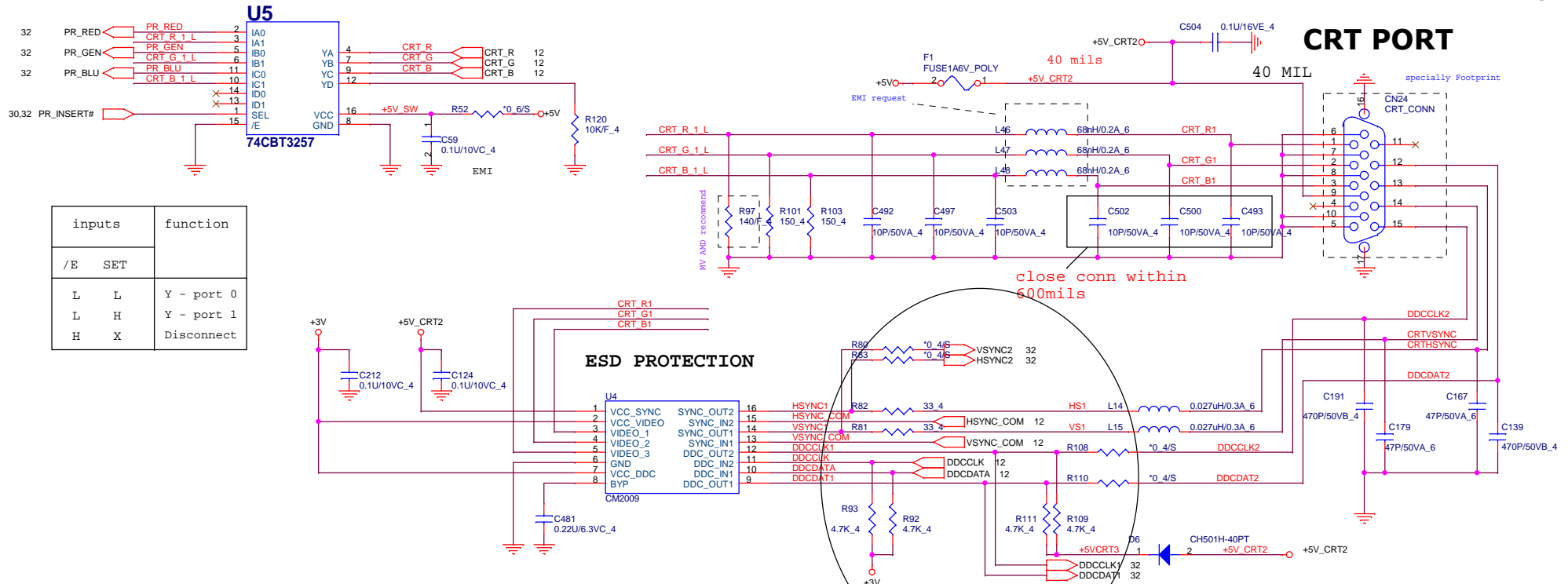
+3VPCU 5,14,25,29,30,32,33,35,37,39
+3V 4,5,7,8,9,12,13,14,15,16,17,18,20,22,23,26,28,29,30,31,33,34,38
+3VSUS 15,21,24,25,29,31,33,34,35,36,38
+5V 17,20,22,23,28,31,32,33,37,38,39
+12VALW 28,31,33,38

Speaker / DMIC
+5VSUS --> Camera
+3V --> Digitizer
Digitizer control signal



PROJECT : TT3
Quanta Computer Inc.

Size Custom	Document Number LCD CONN,HDMI CONN	Rev 1A
Date: Wednesday, August 27, 2008		Sheet 19 of 41



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

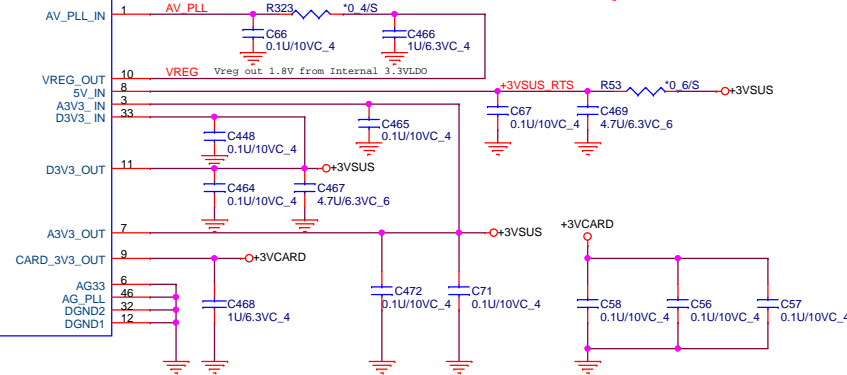
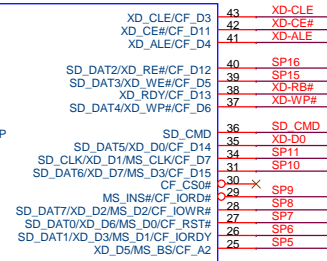
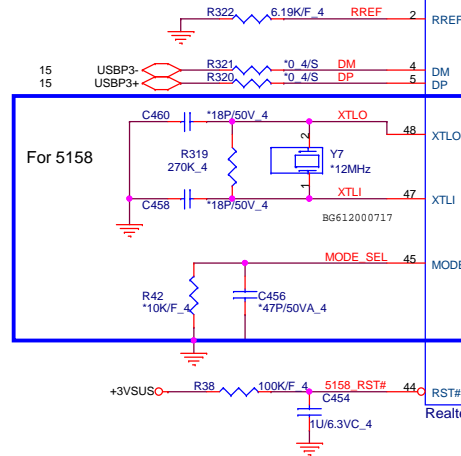
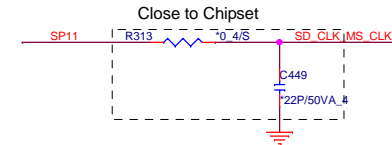
Del S-Video



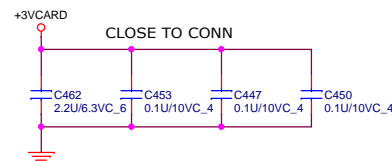
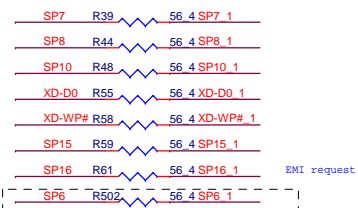
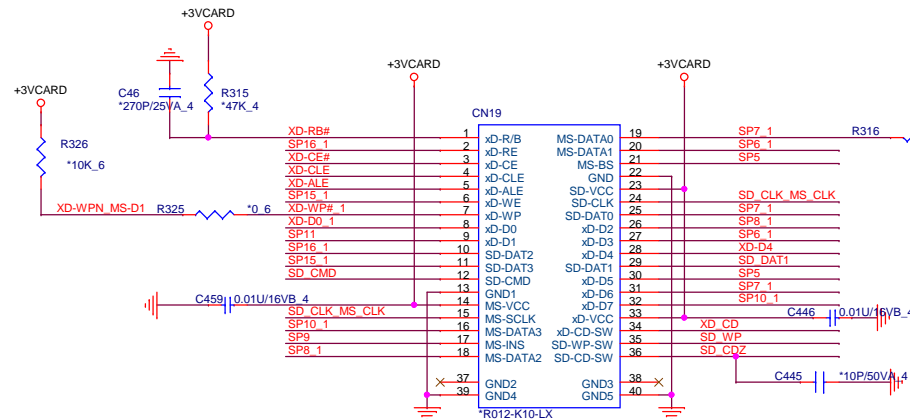
PROJECT : TT3
Quanta Computer Inc.

Size Custom	Document Number CRT_TV_OUT	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 20 of 41	

	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4			XD D4
SP5		MS BS	XD D5
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE



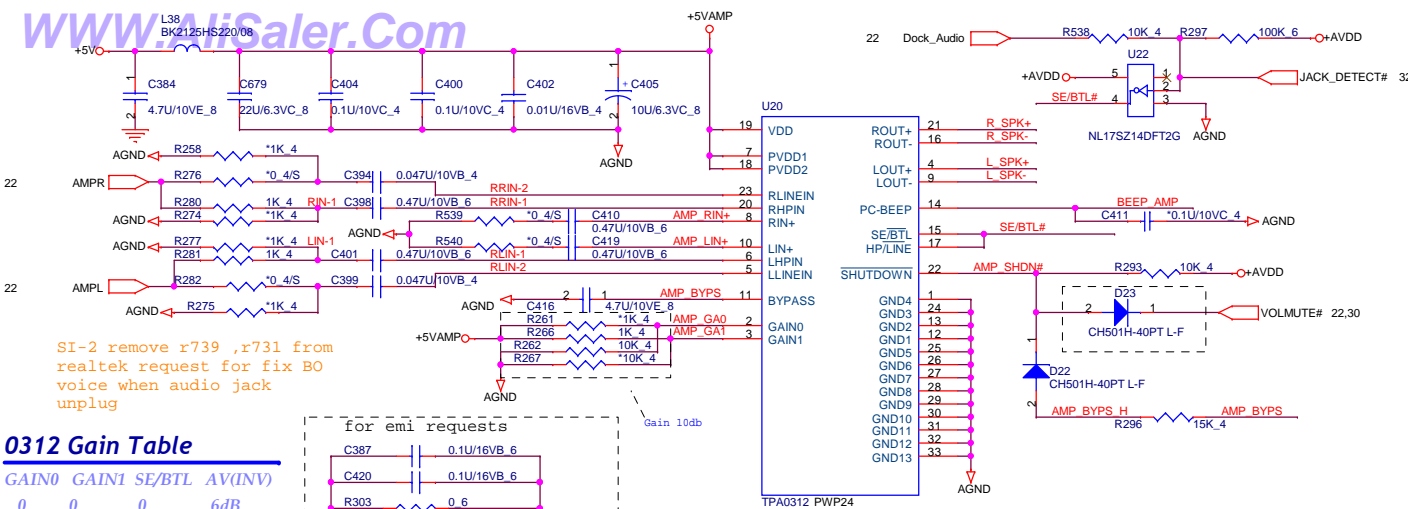
XD,MMC/SD,MS/MSP

[illegible]

➤ +3VSUS 15,24,25,29,31,33,34,35,36,38



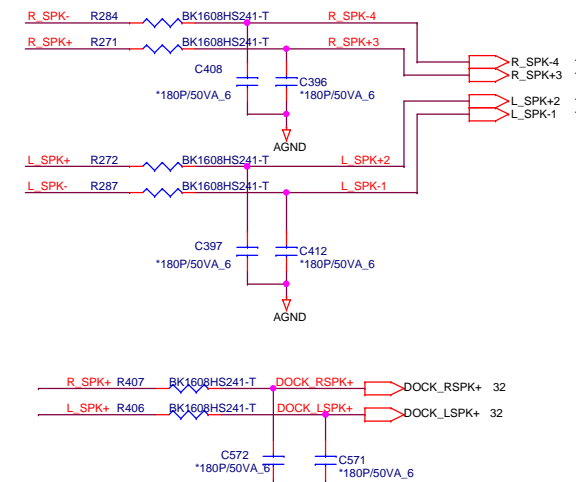
Size Custom	Document Number RT5158 CARD READER CONTROLLER	Rev 1A
----------------	--	-----------



0312 Gain Table

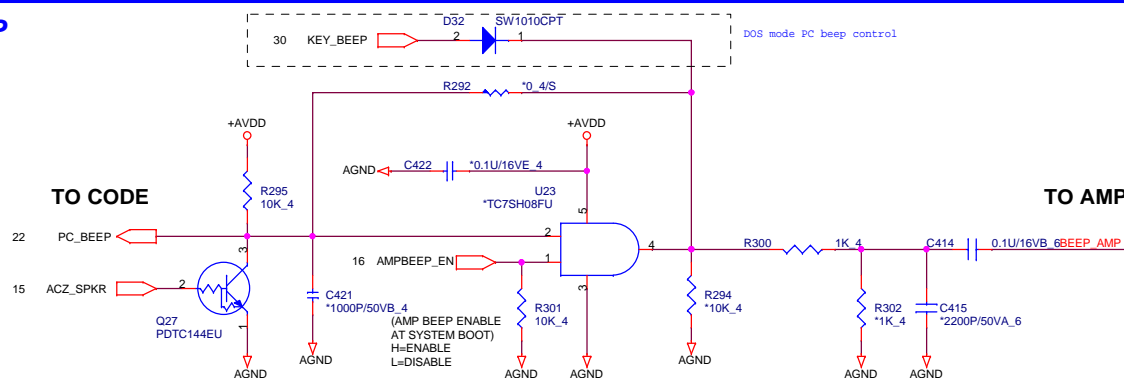
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

INT. SPEAKER

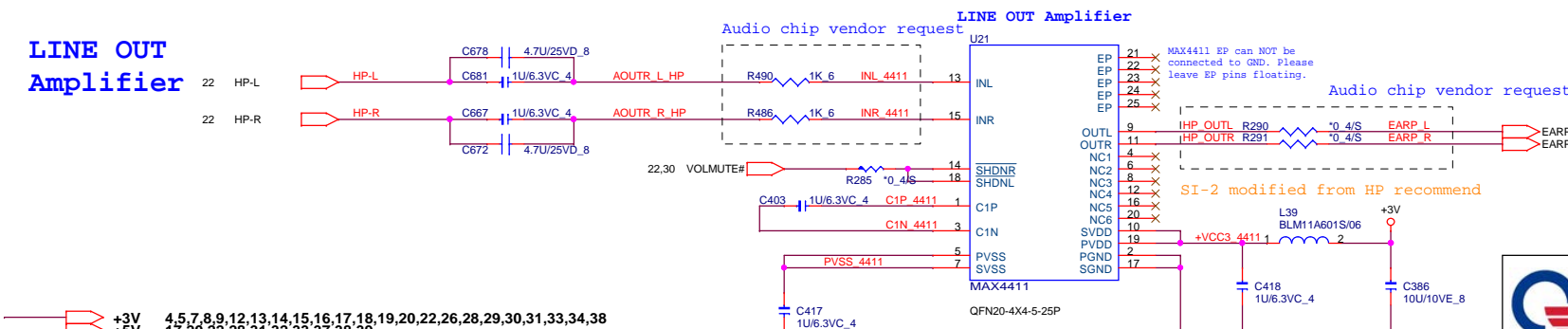


AUDIO AMPLIFIER

PCSPK BEEP

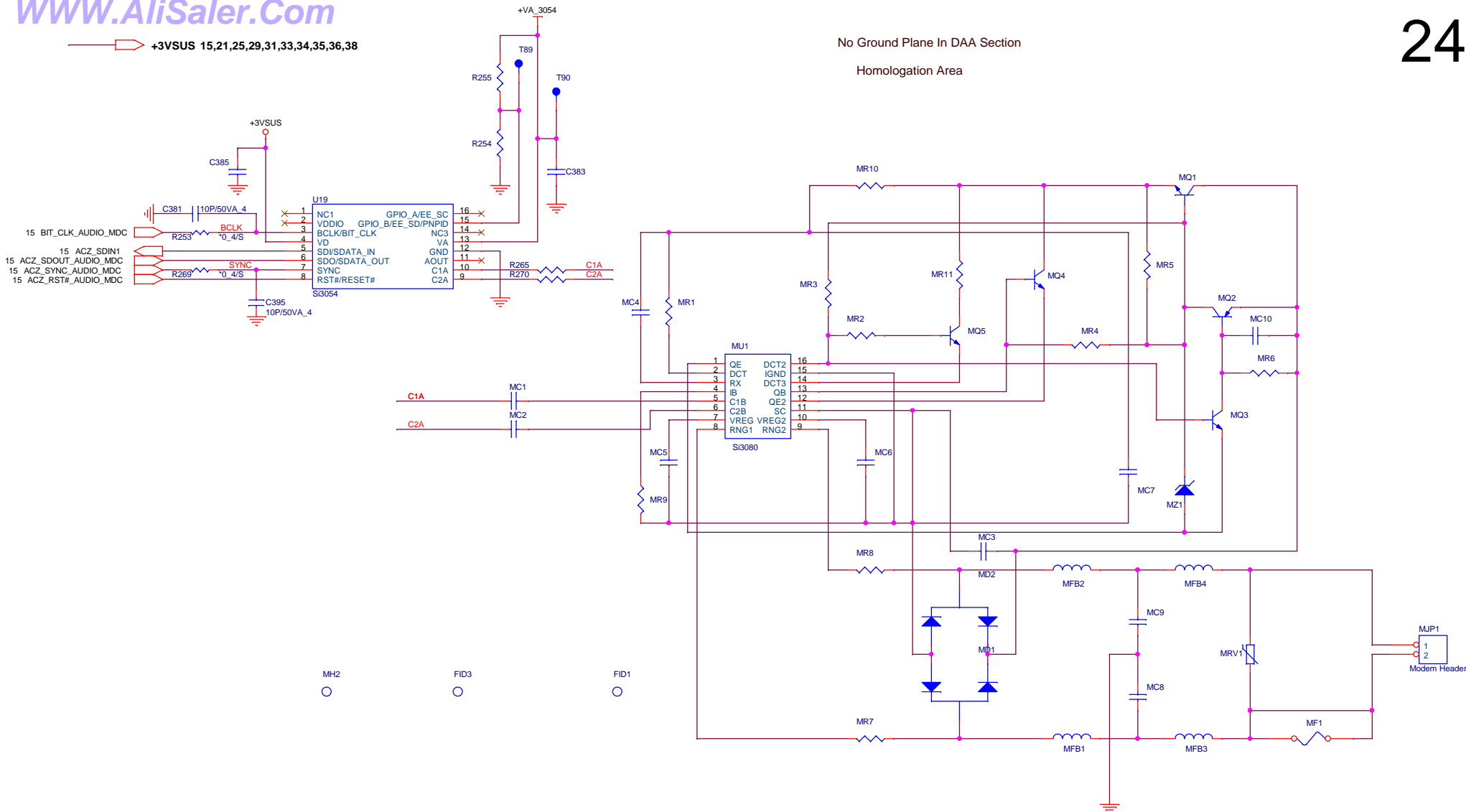


LINE OUT Amplifier



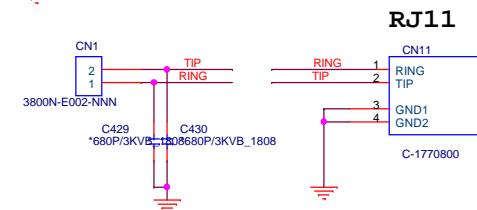
PROJECT : TT3
Quanta Computer Inc.

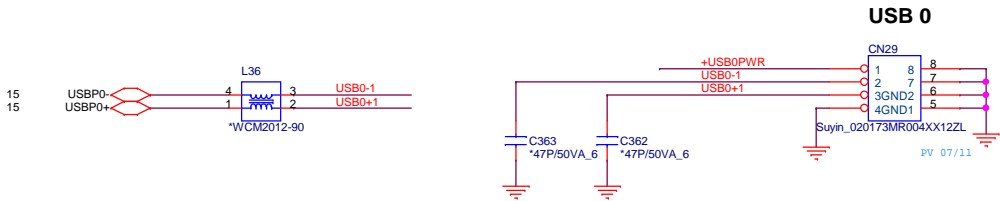
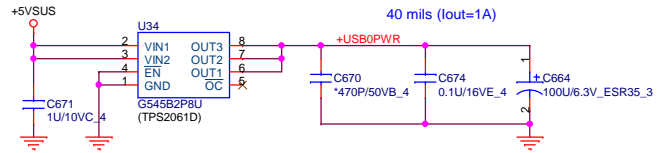
Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A
Date: Wednesday, August 27, 2008	Sheet 23 of 41	



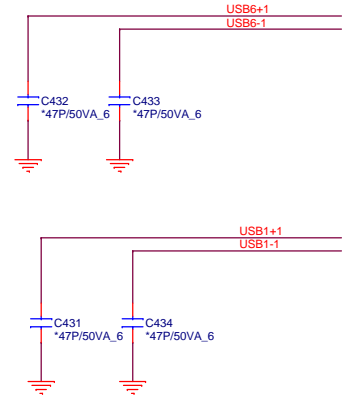
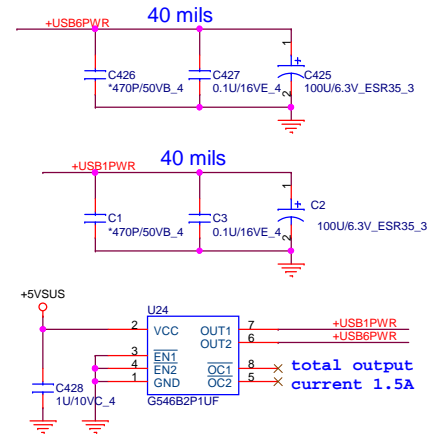
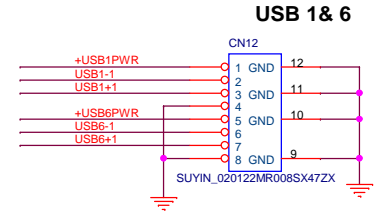
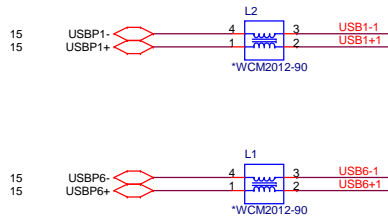
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

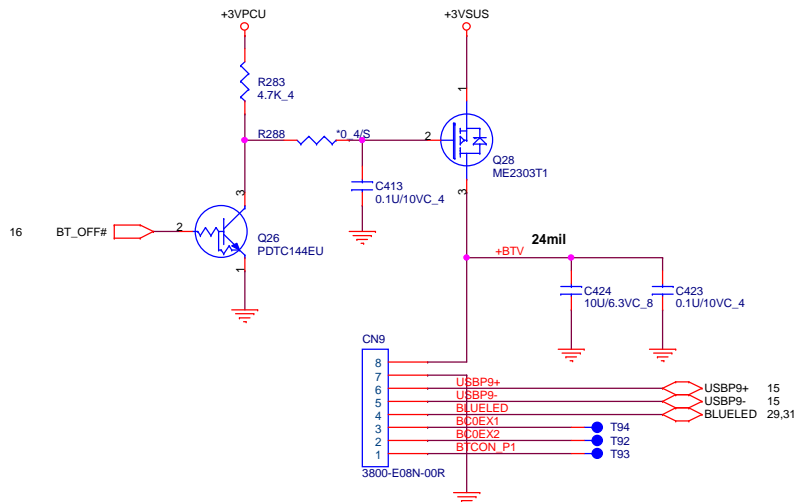




USBX2



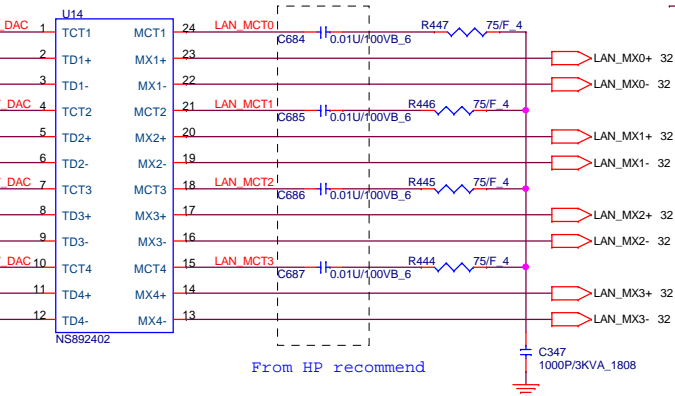
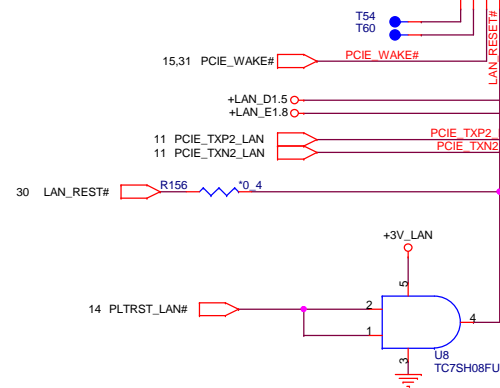
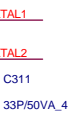
BLUETOOTH



+3VPCU 5,14,19,29,30,32,33,35,37,39
+3VSUS 15,21,24,29,31,33,34,35,36,38
+5VSUS 19,30,32,33,38

for +3VLAVCC > 40mil

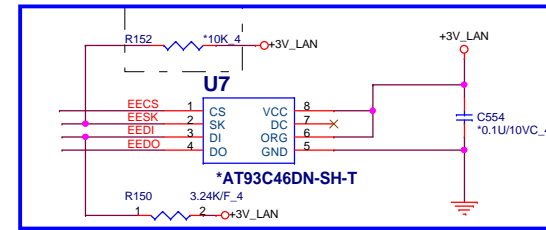
for +CTRL18 > 60mil



From HP recommend

C347 1000P/3KVA_1808

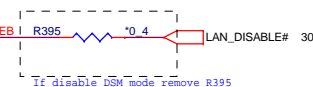
for 93C56 used. NC if 93C46 is used.



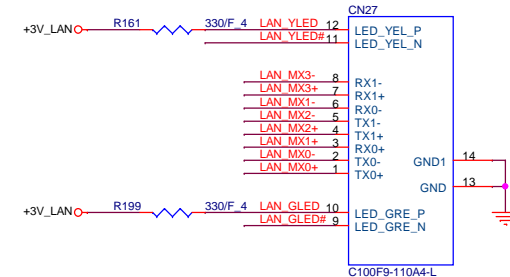
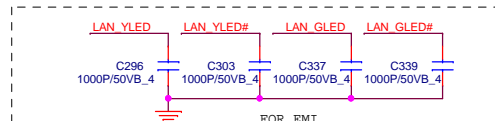
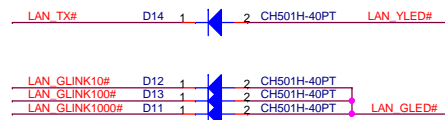
26

Remove LAN EEPROM

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



RJ45

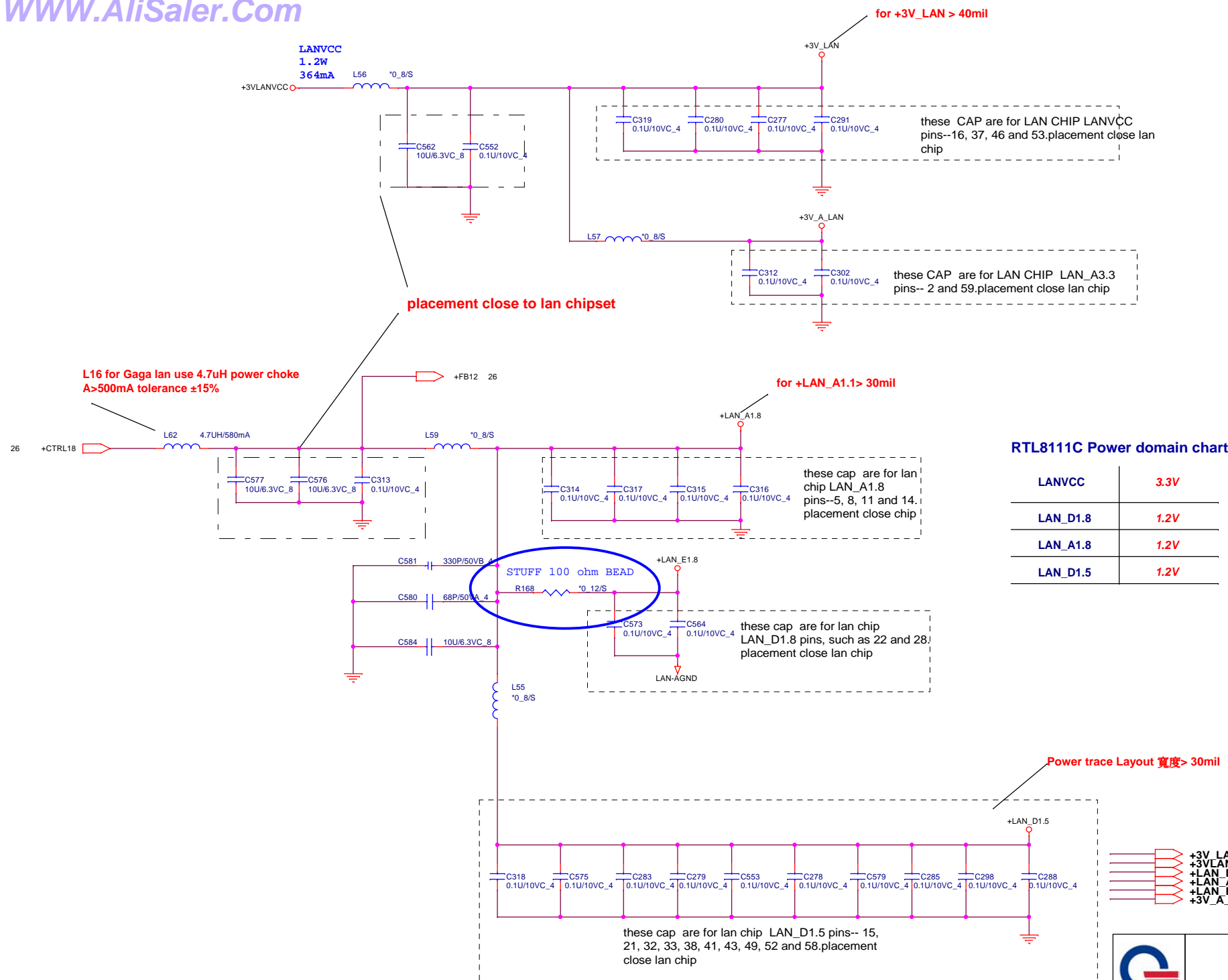


+3V LAN 27
+3VLAVCC 27,33,38
+LAN_D1.5 27
+LAN_A1.8 27

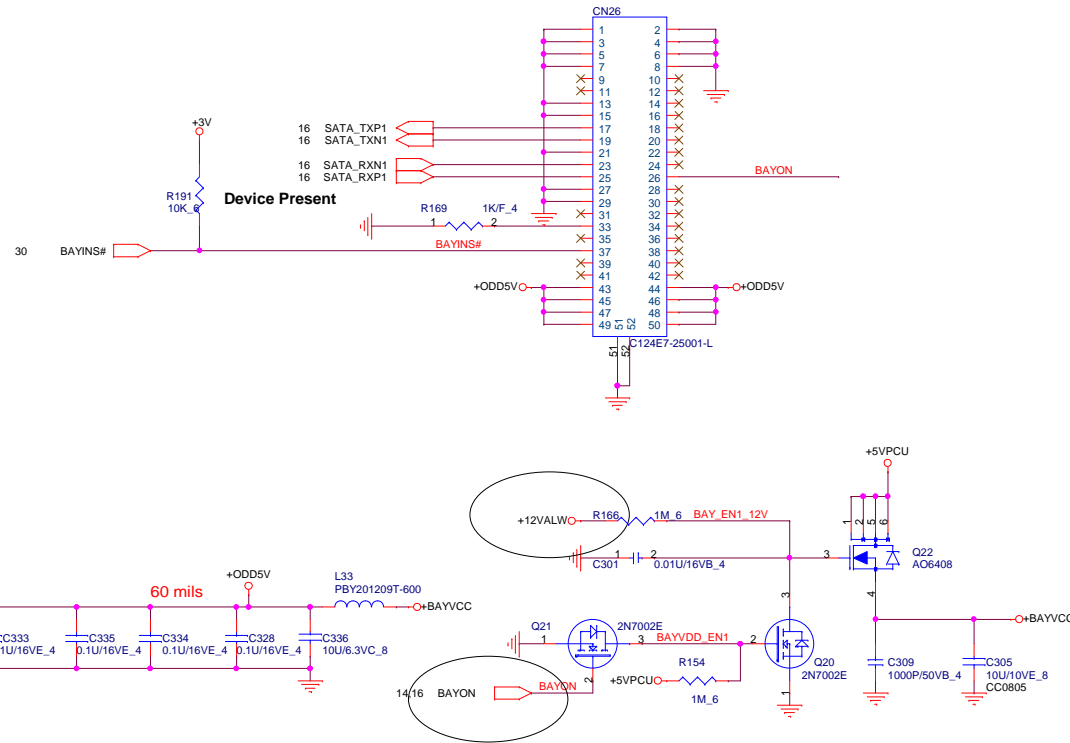


PROJECT : TT3
Quanta Computer Inc.

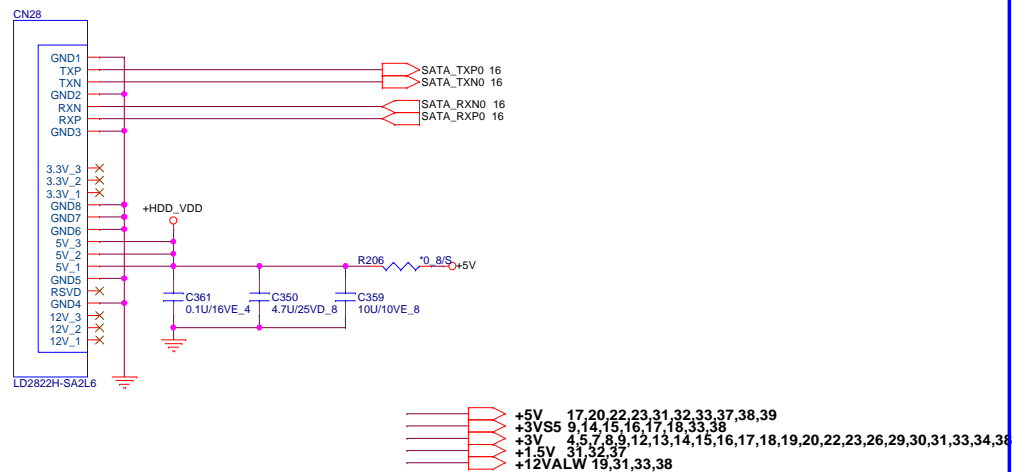
Size Custom	Document Number Pealtek RTL8111C	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 26 of 41	



SATA ODD

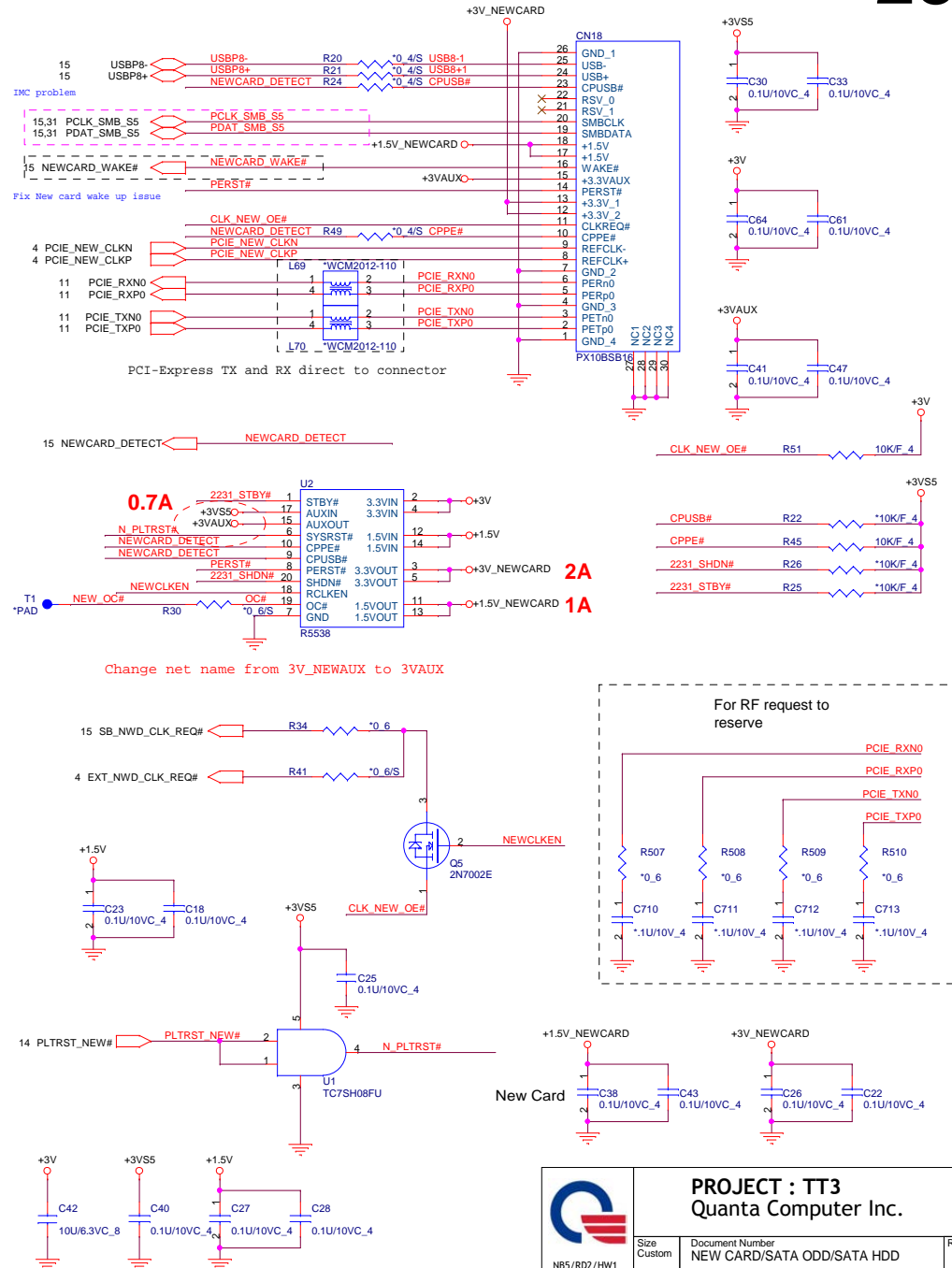


SATA CONNECTOR

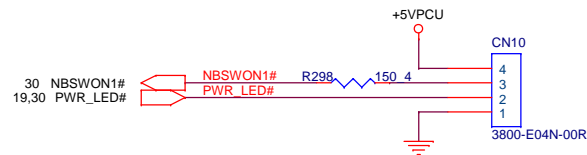
**NEWCARD**

NEWCARD (PCIEXPRESS*1 + USB*1)

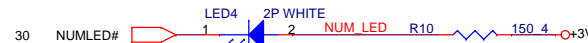
28



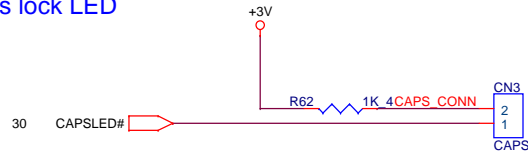
FOR POWER ON SW BOARD



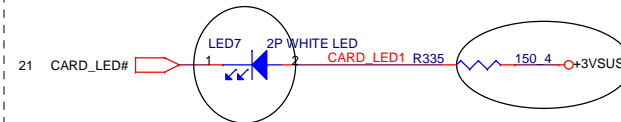
Num lock LED



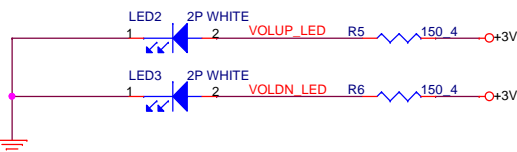
Caps lock LED



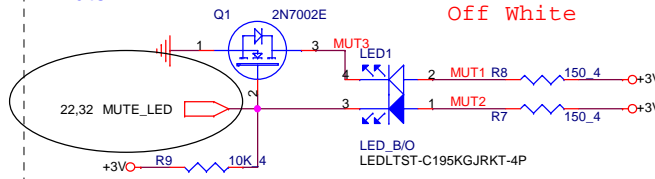
Card Reader LED



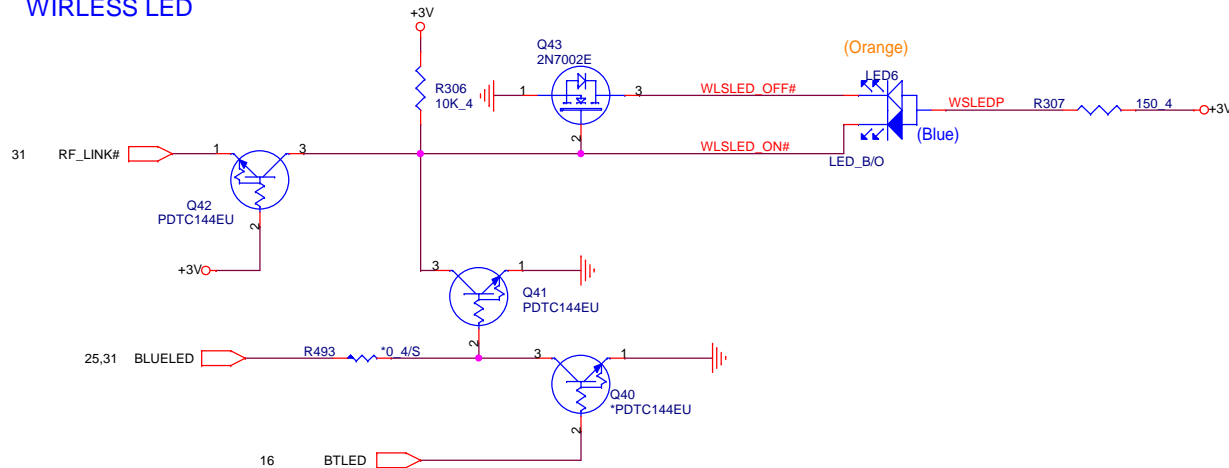
Volume up/down LED



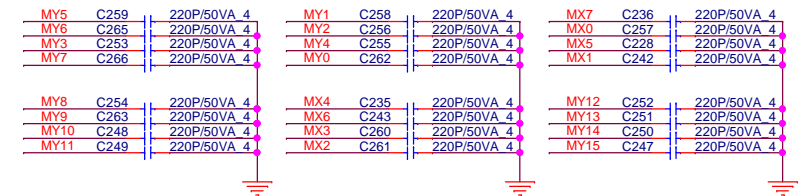
Mute LED



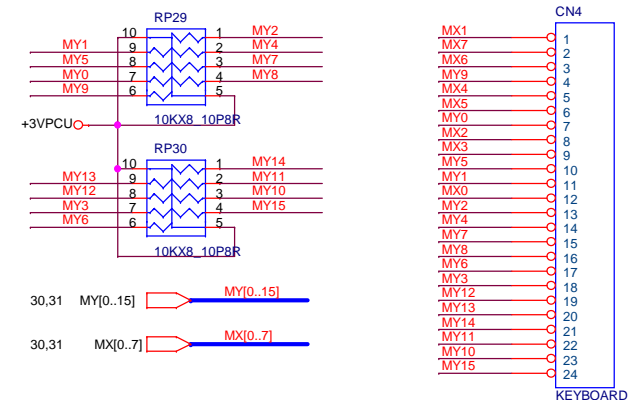
WIRLESS LED



Keyboard



KEYBOARD PULL-UP

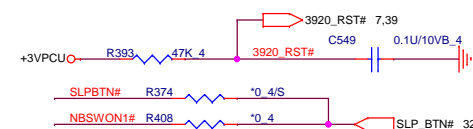
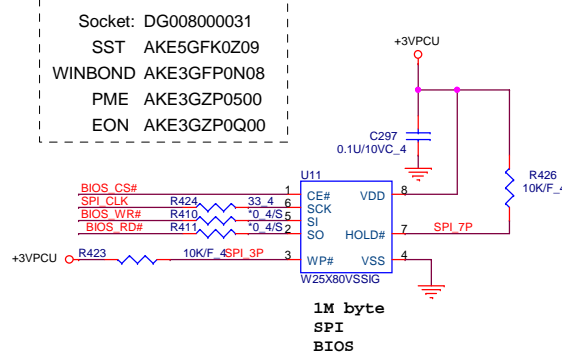
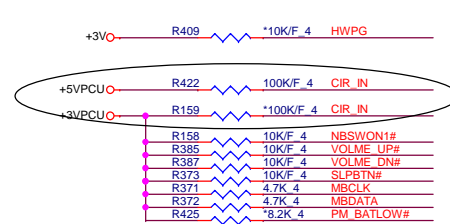
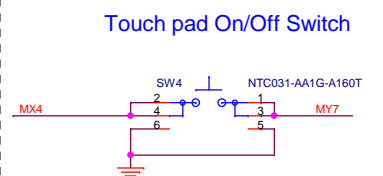
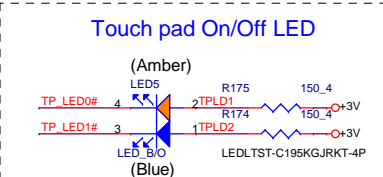
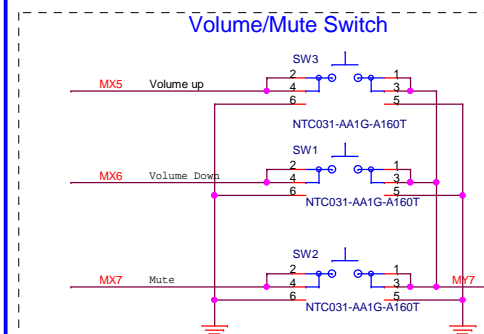
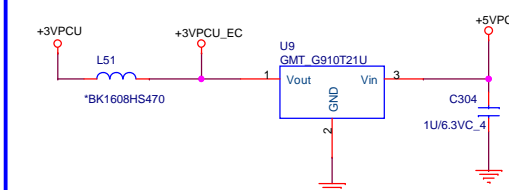
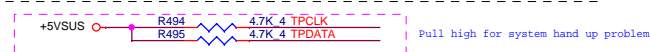
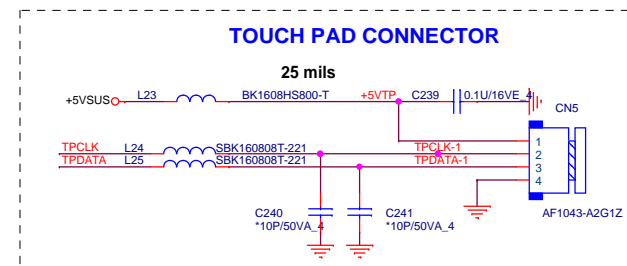
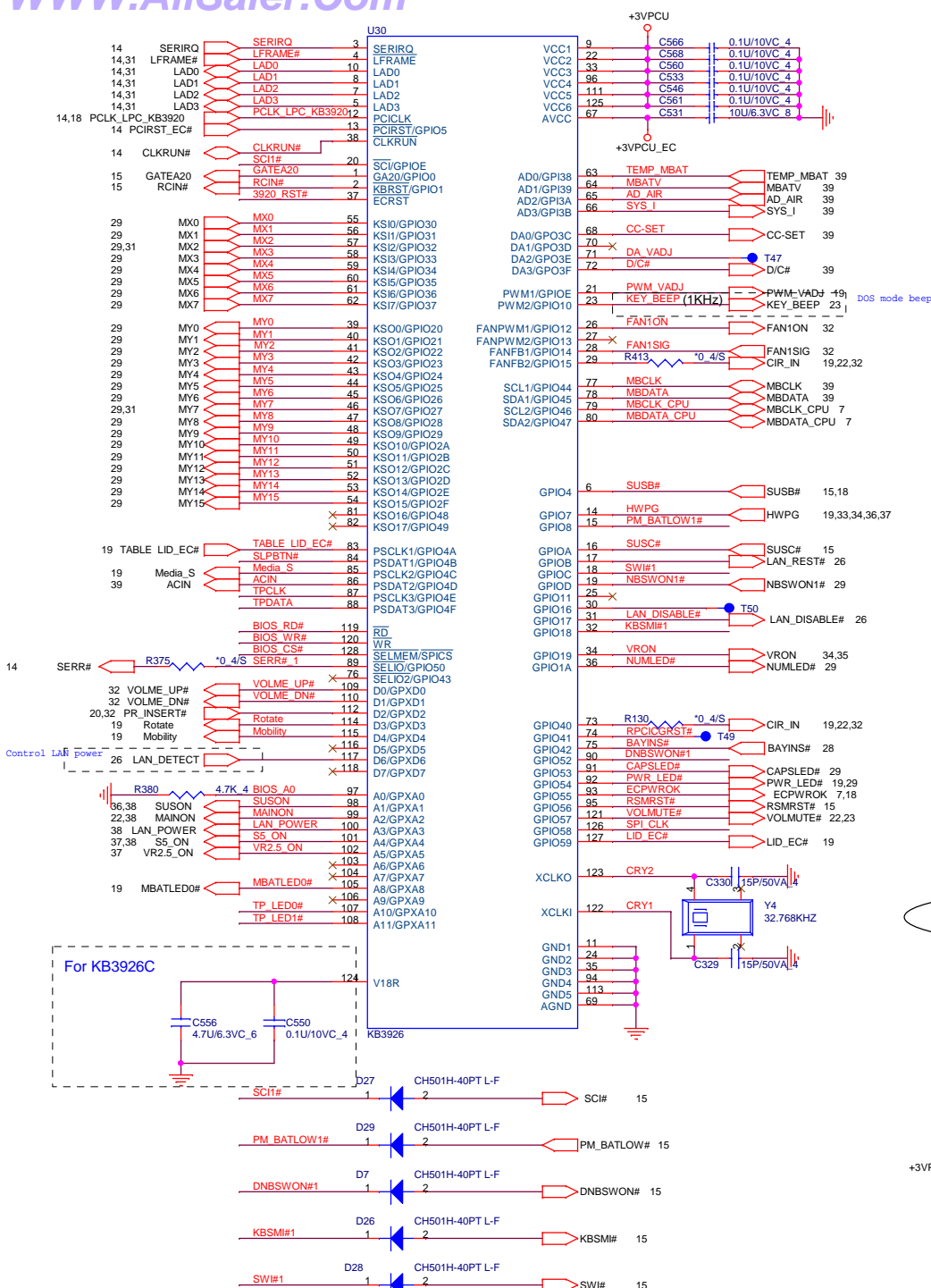


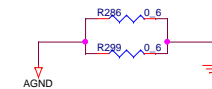
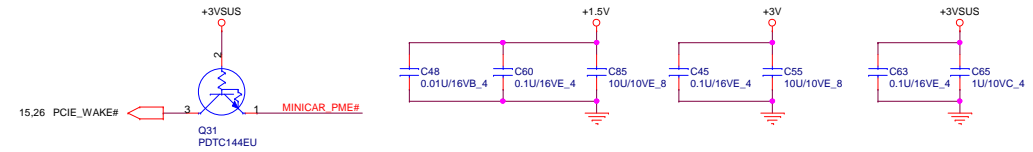
+5VPCU 19,22,28,30,33,34,35,36,37
+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38
+3VSUS 15,21,24,25,31,33,34,35,36,38

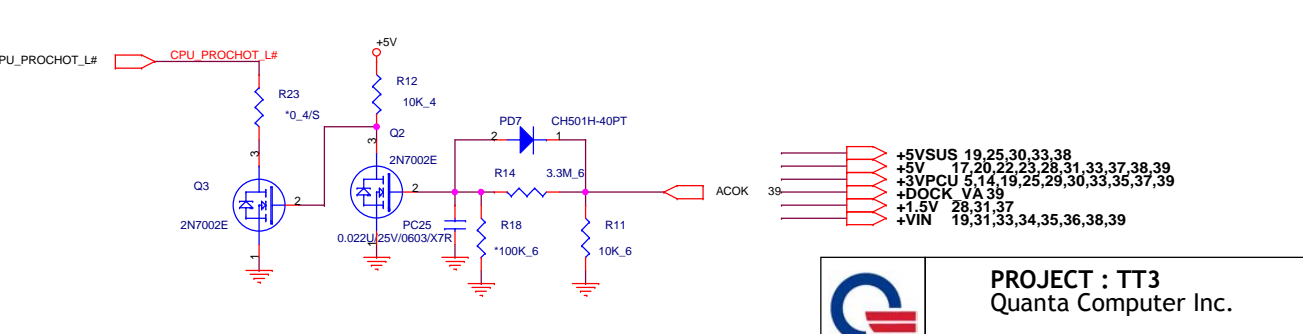
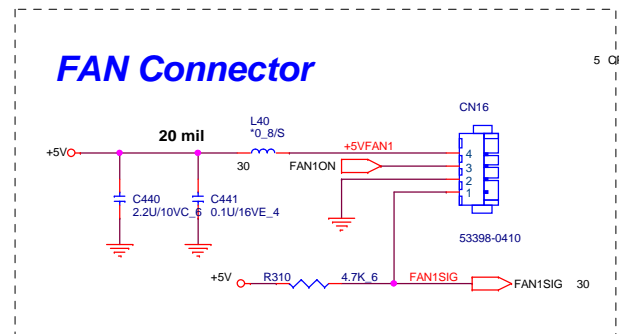
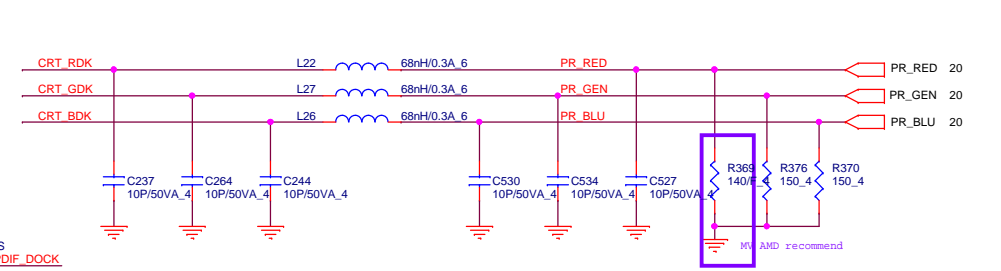
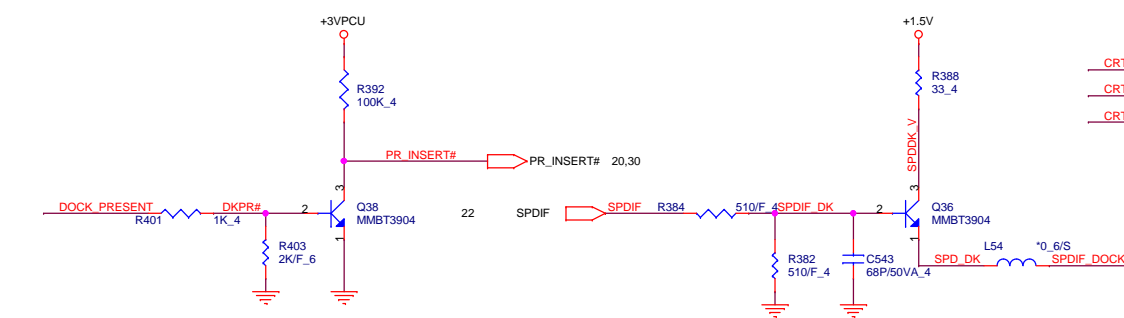
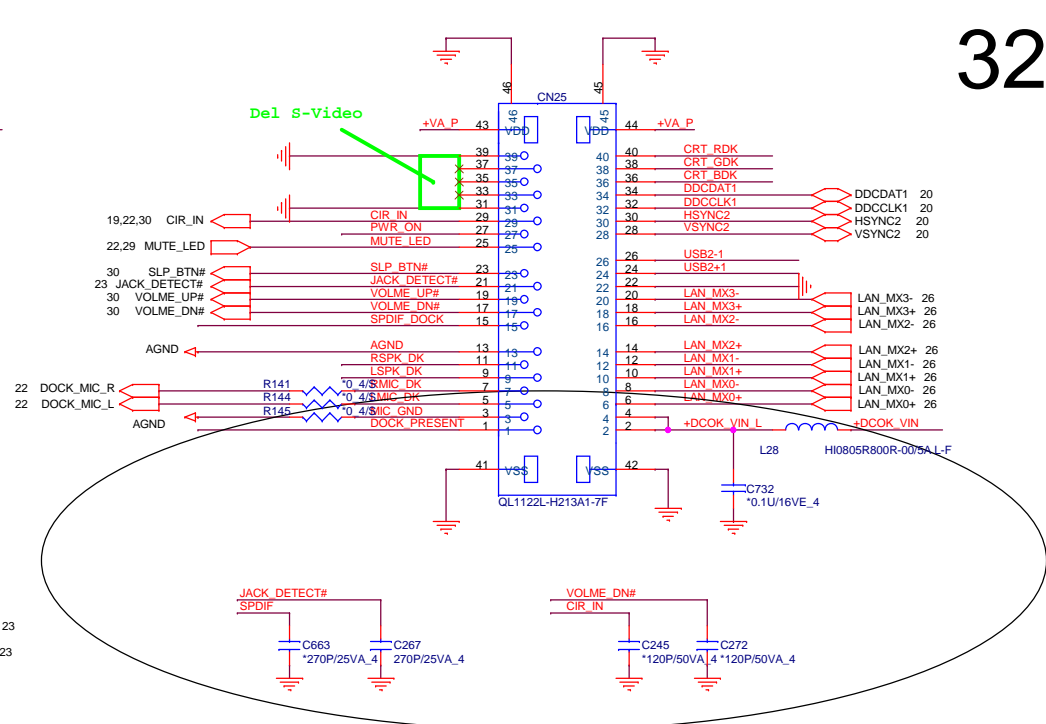
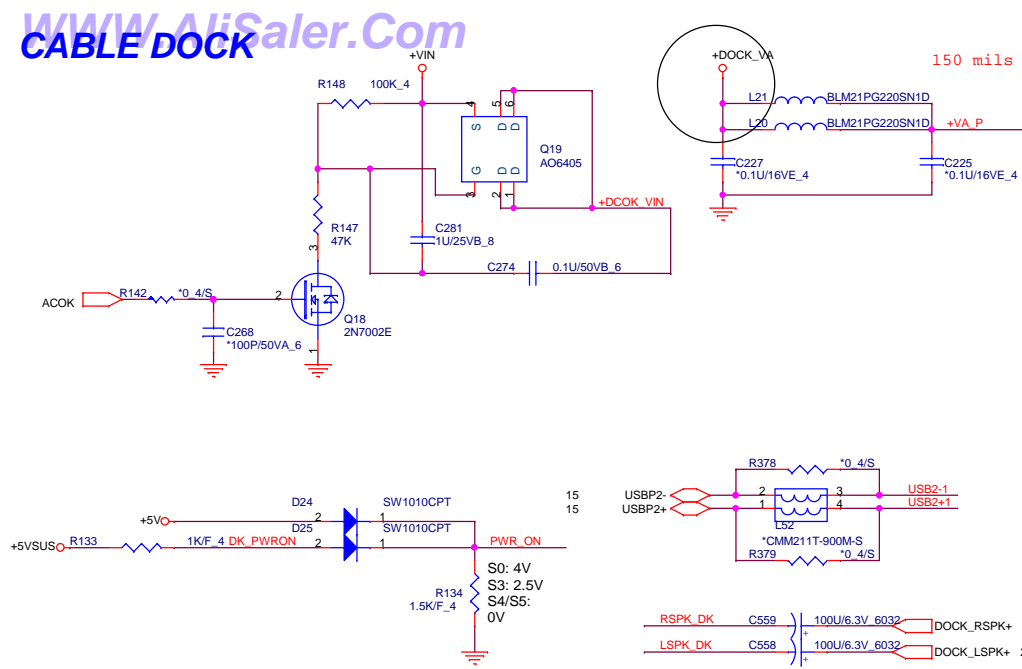


PROJECT : TT3
Quanta Computer Inc.

Size B	Document Number LED/KEYBOARD/SW	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 29 of 41	







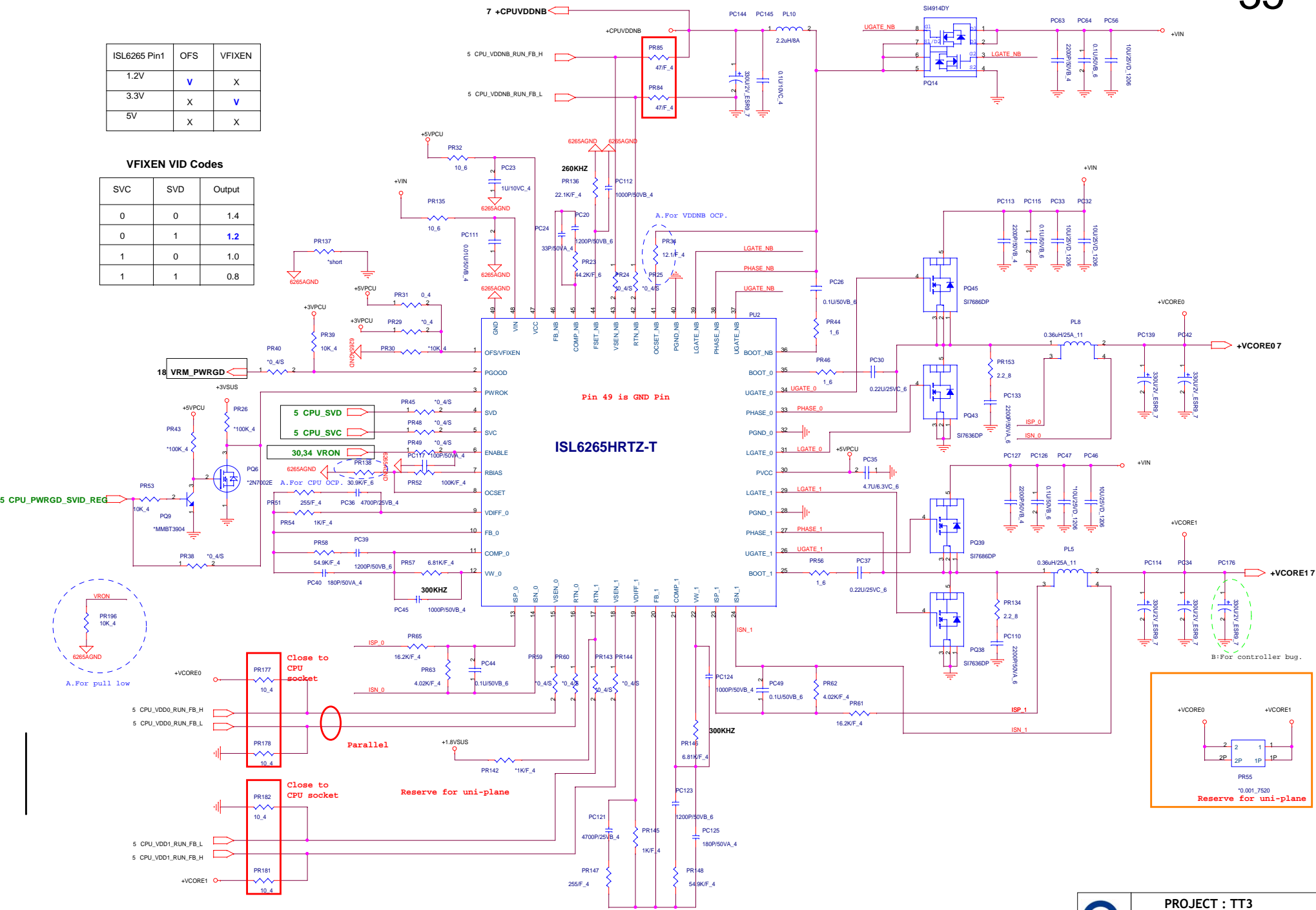


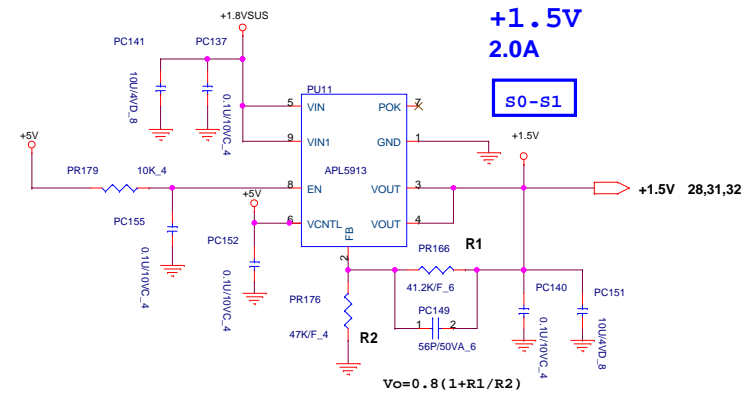
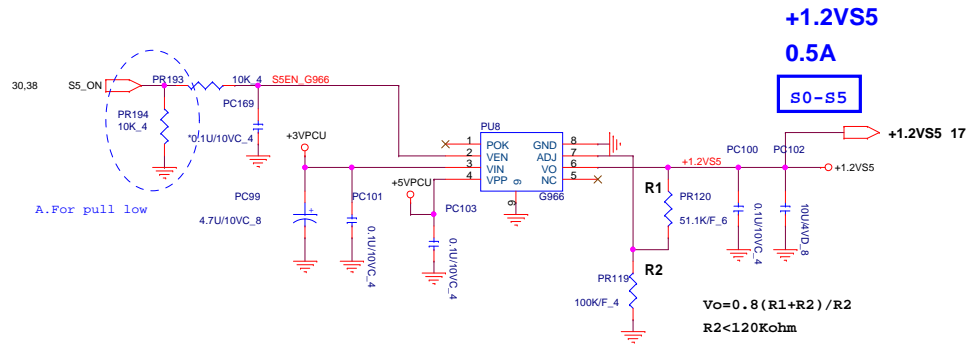
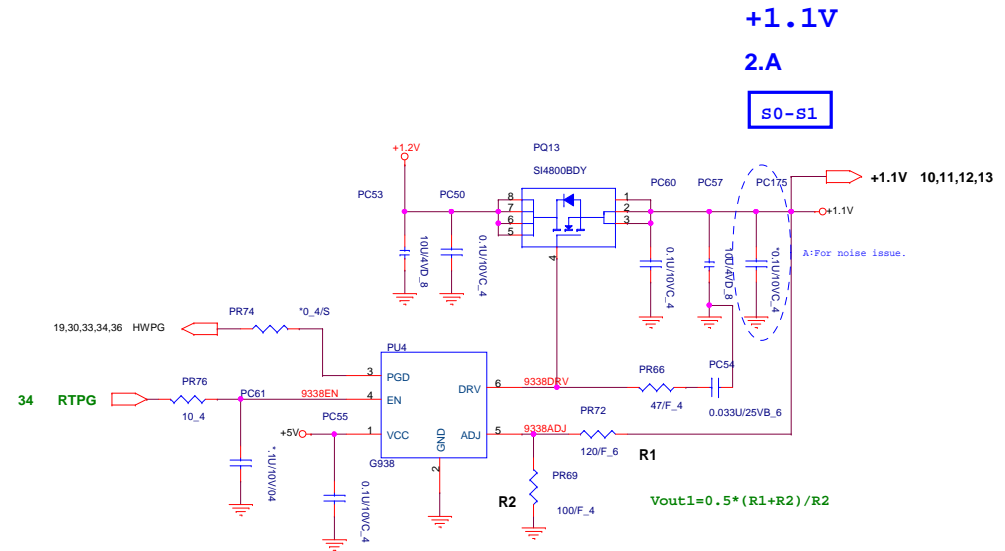
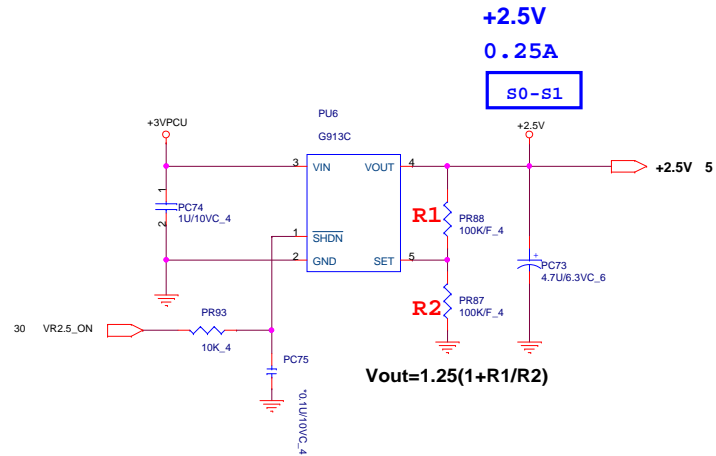


ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

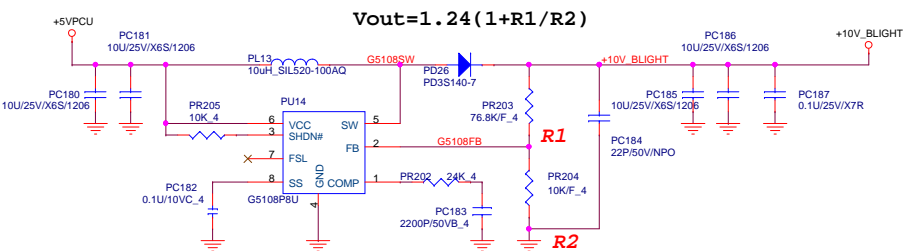
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





Boost 10V



PROJECT : TT3 Quanta Computer Inc.		
Size Custom	Document Number +1.2V_S5/+1.5/+1.1V/+2.5V	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 37 of 41	

